

SEARCH REQUEST FORM

FIGURE 5/10/95

Requestor's Name: ASTA Serial Number: 08/437975
Date: 5/10/96 Phone: 305-3817 Art Unit: 2318

Search Topic: Michele

Please write a detailed statement of search topic. Describe specifically as possible the subject matter to be searched. Define any terms that may have a special meaning. Give examples or relevant citations, authors keywords, etc., if known. For sequences, please attach a copy of the sequence. You may include a copy of the broadest and/or most relevant claim(s).

SYNCHRONOUS DRAM CONTROLLER WHICH
SORTS (REORDERS) Memory Requests based on
their addresses and processing the memory
requests out of order to maximize
throughput

If possible I
need this by very
early afternoon - case
is due and I need
to complete today

Thanks
Bob

A NOTE FROM YOUR EIC/CPAC SEARCHER

It is our sincere desire at the Electronic Information Center/Computer Prior Art Collection to provide you with the most timely, accurate, and comprehensive search results in support of your duties.

If you have any questions about this search, or if you feel that this search has "missed the mark" in meeting your needs -- either in terms of databases selected for searching or the search strategy used -- please contact me as soon as possible so that we can explore ways to improve the precision and recall of these results.

Robert F. (Bob) Jack 308-7795
Technical Information Specialist

STAFF USE ONLY

Date completed: 5/10/96
Searcher: Robert F. Jack
Terminal time: 1:298 - 78 mins
Elapsed time: 22 mins pre & post
CPU time: _____
Total time: 100 minutes
Number of Searches: 1
Number of Databases: 42

Search Site
____ STIC
____ CM-1
____ Pre-S
Type of Search EIC
____ N.A. Sequence
____ A.A. Sequence
____ Structure
____ Bibliographic

Vendors
____ IG Suite
____ STN
____ ✓ Dialog
____ APS
____ Geninfo
____ SDC
____ DARC/Questel
____ Other

in @ 10:10am and 11:50am.

Announcement)
Gwennap, Linley
Microprocessor Report, v8, n12, p1(6)
Sept 12, 1994
DOCUMENT TYPE: Product Announcement
ENGLISH
WORD COUNT: 4773

ISSN: 0899-9341

LANGUAGE:

RECORD TYPE: FULLTEXT

LINE COUNT: 00361

... Stall Processor

The 21164 always issues instructions in order and does not include the extensive *****out*****-of-order execution logic that will be used in other next-generation CPUs. The chip includes limited *****out*****-of-*****order***** execution, however, allowing instructions to continue executing while cache misses are being serviced.

The "merge logic" in Figure 1 includes a six-entry miss *****address***** file (MAF) that captures information on loads that miss the data cache. Once the integer unit generates the *****address***** for a load, it is finished with that instruction and can continue to accept new
...

...is loaded into the register file.

If a load misses the data cache, the load *****address***** and target register are recorded in the MAF, which acts as a FIFO buffer. If... although no peripherals currently support 64-bit PCI. The chip set allows either standard or *****synchronous***** *****DRAM***** for main memory; with the latter chips, the need for an external cache is reduced...

File 752:Datapro Product Specifications 1996/Apr
(c) 1996 McGraw-Hill, Inc.
File 751:Datapro Software Directory 1996/Mar
(c) 1996 McGraw-Hill, Inc.
File 237:Buyer's Guide to Micro Software(SOFT) 1993/Sep
(c) 1993 ONLINE Inc.
File 256:SoftBase:Reviews,Companies&Prods. 95-1996/Mar
(c)1996 Info.Sources Inc
File 278:Microcomput.Software Guide 1996/Apr
(c) 1996 Reed Reference Publishing

Set	Items	Description
S1	0	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACC- ESS() (MEMORY OR MEMORIES))))
S2	0	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMM- AND? ? OR MEMORY()REQUEST? ?)
S3	138	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	0	S1 AND S3
S6	460	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	0	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8
S10	64	DRAM OR (DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMOR- IES)))
S11	0	S2 AND S10
S12	0	S3 AND S10
S13	0	S6 AND S10

File 351:DERWENT WPI 1981-1996/UD=9618;UA=9614;UM=9606
 (c)1996 Derwent Info Ltd
 File 350:Derwent World Pat. 1963-1980/UD=9616
 (c) 1996 Derwent Info Ltd
 File 348:EUROPEAN PATENTS 1978-1996/MAY W1
 (c) 1996 European Patent Office
 File 347:JAPIO OCT 1976-1995/DEC.
 (c) JPO & JAPIO
 File 344:Chinese Patents ABS Apr 1985-1996/Apr
 (c) 1996 European Patent Office

Set	Items	Description
S1	113	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACC- ESS() (MEMORY OR MEMORIES))))
S2	6	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMM- AND? ? OR MEMORY()REQUEST? ?)
S3	917	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	0	S1 AND S3
S6	2719	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	324	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8
S10	9389	DRAM OR DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORI- ES))
S11	0	S10 AND S2
S12	0	S10 AND S3
S13	1	S10 AND S6

13/5/1 (Item 1 from file: 348)
 DIALOG(R) File 348:EUROPEAN PATENTS
 (c) 1996 European Patent Office. All rts. reserv.

00185318

Microprocessor and *****dynamic***** *****RAM***** system with software refreshment, application to a disturbance recorder.

PATENT ASSIGNEE:

Artus, Societe Anonyme, (1119170), Chemin du Champ des Martyrs, F-49240
 Avrille, (FR), (applicant designated states:
 AT;BE;CH;DE;GB;IT;LI;LU;NL;SE)

AUTHOR (Inventor):

Pastre, Jean-Luc, THOMSON-CSF SCPI 173, bld Haussmann, F-75379 Paris
 Cedex 08, (FR)

LEGAL REPRESENTATIVE:

Thevenet, Jean-Bruno et al (39781), Cabinet BEAU DE LOMENIE 55 rue
 d'Amsterdam, F-75008 Paris, (FR)

PATENT (CC, No, Kind, Date): EP 156722 A1 851002 (Basic)
 EP 156722 B1 900620

APPLICATION (CC, No, Date): EP 85400474 850312;

PRIORITY DATA (CC, No, Date): FR 844105 840316

LANGUAGE (Publication,Procedural,Application): French; French; French

DESIGNATED STATES: AT; BE; CH; DE; GB; IT; LI; LU; NL; SE

INTL PAT CLASS: G11C-011/24;

CITED PATENTS (EP A): US 4204254 A; EP 94042 A

CITED REFERENCES (EP A)

IBM TECHNICAL DISCLOSURE BULLETIN, vol. 24, no. 10, mars 1982, pages
 4983-4984, New York, US; C.E. BOYD et al.: "Software/hardware approach

to dynamic memory refresh";
WORD COUNT: 162

ABSTRACT: EP 156722 A1

Système a microprocesseur et memoire vive dynamique avec rafraichissement par logiciel, application a un enregistreur de perturbations.

L'invention concerne les systemes informatiques utilisant un ou plusieurs microprocesseurs (1) ayant acces a une memoire vive dynamique (6). Elle permet le rafraichissement de la memoire dynamique sans l'utilisation de circuits complexes et speciaux a cette operation.

Lors des acces a la memoire morte (5), les adresses des pas du programme stocke en memoire morte, issues de la sortie du compteur ordinal (9) du microprocesseur (1), sont utilisees pour constituer les adresses des rangees de la memoire vive a rafraichir. Cette derniere est ainsi rafraichie regulierement par le logiciel du systeme.

La commande de la memoire est assuree par un sequenceur (8) lui-meme commande par un generateur d'horloge (3) et le microprocesseur. Un multiplexeur (7) est utilise pour adresser la memoire vive.

Application aux systemes de controle ou de surveillance de grandeurs, utilisant plusieurs microprocesseurs, et en particulier, a un enregistreur de perturbations.

LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	851002	A1	Published application (A1withSR;A2withoutSR)
Examination:	860521	A1	Date of filing of request for examination: 860319
Examination:	881026	A1	Date of despatch of first examination report: 880908
*Assignee:	890524	A1	Applicant (name, address) (change)
Change:	890830	A1	Representative (change)
*Assignee:	890830	A1	Applicant (transfer of rights) (change): Artus, Societe Anonyme (1119170) Chemin du Champ des Martyrs F-49240 Avrille (FR) (applicant designated states: AT;BE;CH;DE;GB;IT;LI;LU;NL;SE)
*Assignee:	890830	A1	Previous applicant in case of transfer of rights (change): THOMSON-CSF (201769) 51, Esplanade du General de Gaulle F-92800 Puteaux (FR) (applicant designated states: AT;BE;CH;DE;GB;IT;LI;LU;NL;SE)
Grant:	900620	B1	Granted patent
Lapse:	910320	B1	Date of lapse of the European patent in a Contracting State: SE 900620
Lapse:	910502	B1	Date of lapse of the European patent in a Contracting State: NL 900620, SE 900620
Oppn None:	910612	B1	No opposition filed

File 351:DERWENT WPI 1981-1996/UD=9618;UA=9614;UM=9606

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File 350:Derwent World Pat. 1963-1980/UD=9616

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File 348:EUROPEAN PATENTS 1978-1996/MAY W1

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File 347:JAPIO OCT 1976-1995/DEC.

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File 344:Chinese Patents ABS Apr 1985-1996/Apr

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Set	Items	Description
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S4	0	S1 AND S2
S5	0	S1 AND S3
S6	2719	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	324	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8
S10	9389	DRAM OR DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORIES))
S11	0	S10 AND S2
S12	0	S10 AND S3
S13	1	S10 AND S6
S14	3	S10 AND S8
S15	3	S14 NOT S13

15/5/1 (Item 1 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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009091383 WPI Acc No: 92-218806/27

XRPX Acc No: N92-166148 *Image available*

*****DRAM***** with voltage stress testing - transfers voltage applied to test pad by transistors to word lines selected by external address with noise killer circuit turned off; *****DYNAMIC***** *****RAM*****

Patent Assignee: (TOKE) TOSHIBA KK

Author (Inventor): KOYANAGI M; TANAKA H

Number of Patents: 003

Number of Countries: 005

Patent Family:

CC Number	Kind	Date	Week	
EP 492610	A1	920701	9227	(Basic)
JP 4230047	A	920819	9240	
US 5255229	A	931019	9343	

Priority Data (CC No Date): JP 90418761 (901227)

Applications (CC,No,Date): US 813578 (911226); EP 91122192 (911223)

Language: English

EP and/or WO Cited Patents: DE 3932442; US 4751679; US 4922453

Designated States

(Regional): DE; FR; GB

Abstract (Basic): EP 492610 A

The memory has a voltage stress test pad (22) to which a stress voltage is externally applied when a test is carried out with transistors (24) which turn off when a voltage is not applied. These transmit the stress voltage to more word lines than those selected in response to an external address signal in normal operation mode with a noise killer circuit (38).

This circuit controls the noise killer circuit and turns off the circuit (24) connected to a word line to which the stress voltage test is carried out.

ADVANTAGE - Improved screening with greater efficiency.

Dwg.1/1

Abstract (US): 9343 US 5255229 A

The *****dynamic***** *****random***** *****access*****
*****memory***** has a voltage stress test pad to which a stress voltage is externally applied when a voltage stress test is carried *****out*****. Transistors *****turn***** off when the stress voltage is not applied to the voltage stress test pad and which, when the stress voltage is applied thereto, transmit the stress voltage to more word lines than those selected in response to an external *****address***** signal in a normal operation mode.

A noise killer control circuit for turning off a noise killer circuit is connected to a word line to which the stress voltage is applied when the voltage stress test is carried out.

USE - In defect screening in wafer production.

Dwg.1/1

File Segment: EPI

Derwent Class: U13; U14;

Int Pat Class: G01R-031/318; G11C-007/02; G11C-029/00; H01L-021/66

Manual Codes (EPI/S-X): U13-C04B1A; U14-A07; U14-D

.15/5/2 (Item 2 from file: 351)

DIALOG(R)File 351:DERWENT WPI

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007001230 WPI Acc No: 87-001227/01

XRPX Acc No: N87-000985

Computer memory with semiconductor elements operating system has double fetch capability from word-wide stacks using timer to control of chips

Patent Assignee: (HONE) HONEYWELL INFORM SYSTEMS INC; (HONE) BULL HN
INFORMATION SYSTEMS INC

Author (Inventor): NG A W; FISHER E P

Number of Patents: 010

Number of Countries: 011

Patent Family:

CC Number	Kind	Date	Week	
EP 207504	A	870107	8701	(Basic)
AU 8659395	A	870108	8714	
ZA 8604834	A	870102	8717	
ES 8801462	A	880301	8816	
US 4739473	A	880419	8818	
US 4761730	A	880802	8833	
CA 1262492	A	891024	8948	
EP 207504	B	901122	9047	
DE 3675699	G	910103	9102	
KR 9309668	B1	931008	9437	

Priority Data (CC No Date): US 751179 (850702); US 793047 (851030)

Applications (CC,No,Date): KR 865342 (860702); EP 86108985 (860702); ES 556687 (860625)

Language: English

EP and/or WO Cited Patents: A3...8841; US 3796996; US 4099253; US 4138720;
US 4323965; US 3099253

Designated States

(Regional): DE; FR; GB; IT; SE

Abstract (Basic): EP 207504

The apparatus includes decoders coupled to a set of word blocks of RAM chips on a single circuit board constituting a number of addressable single word wide stacks. The decoders are also coupled to a single word bus for receiving least and most significant bits with an input density signal and for generating a set of select signals to preselect a set of word blocks. A selector coupled to the chips receives at least one L.s.b. and the input density signal.

A timer coupled to the stacks, the selector and a set of registers commonly coupled to the stacks, generates a sequence of timing signals for each of a set type of read operation. The timing signals are applied by the selector to groups of chips related to the set of word blocks to read out from them in tandem.

@(37pp Dwg.No 4/7)@

Abstract (US): 8833 US 4761730

The memory subsystem includes a single addressable memory module unit or stack having a number of word blocks of *****dynamic*****
*****random***** *****access***** *****memory***** (*****DRAM*****)
chips mounted on a single circuit board which connects to the remainder of the subsystem through a single word wide interface. Chip select circuits preselect a pair of blocks of RAM chips from the stack. Timing circuits generate a number of sequential column address pulses which are selectively applied to the preselected blocks of chips within an interval defined by a row *****address***** pulse.

This results in the sequential read out of a pair of words from the preselected blocks of the single word wide module into a pair of subsystems data registers. For each memory read request, the words from each preselected pair of blocks are read *****out***** in
*****sequence***** providing a double fetch capability without any loss in system performance.

ADVANTAGE - Provides double fetch memory subsystem which is implemented with minimum of circuits. @(11pp)@ 8818 US 4739473

The subsystem includes a number of addressable memory module units or stacks each having a number of word blocks of *****dynamic*****
*****random***** *****access***** *****memory***** (*****DRAM*****)
chips arranged in one of two subsystem configurations and mounted on a single circuit board which connects to the remainder of the subsystem through a single word wide interface. The configurations correspond to a common stack arrangement which provides double the normal amount of density and an adjacent stack arrangement of normal density. As a function of an input density signal, chip select circuits preselect a pair of blocks of RAM chips from a common stack or pair of adjacent stacks. Timing circuits generate a number of sequential column address pulses which are selectively applied to the preselected blocks of ships within an interval defined by a row address pulse.

This results in the read out of a pair of words from the preselected blocks of a single stack or adjacent stacks in tandem into a pair of subsystem data registers. For each memory read request, the words from each preselected pair of blocks are read out into the data registers in the same sequence.

ADVANTAGE - Provides double fetch capability without any less in system performance. @(12pp

Abstract (EP): 9047 EP 207504

A memory subsystem coupled to a system bus, wherein said subsystem receives memory access requests from said bus, each request including a

multibit memory address comprising first and second address portions, wherein said subsystem comprises a plurality of blocks of single word wide random access memory chips (word blocks 0-7), a decoder (10-4A) coupled to said blocks of chips for receiving a plurality of at least significant bits of said address and responsive to the bits received thereby to preselect a group of said blocks, a selector (10-6A, 6B, 6C, 6D) coupled to said blocks to receive at least one of said least significant bits, a plurality of registers (10-12, 10-14) coupled in common to said blocks, and timing means (10-10) for generating a sequence of timing signals in response to each request, said subsystem being characterised by said bus comprising a single-word data bus, said timing means being coupled to said blocks, to said selector and to said plurality of registers, a first one of said timing signals conditioning said preselected group of blocks to store and first address portion and second and third ones of said timing signals conditioning said selector to cause each block to store said second address portion for read-out of words from only said preselected group of blocks in a predetermined sequence to said plurality of registers and accessing the group of blocks having been selected by said first and second address portion.

@(16pp)@

File Segment: EPI

Derwent Class: T01; R27;

Int Pat Class: G06F-012/04; G11C-008/00; H03K-019/20

Manual Codes (EPI/S-X): T01-H01A

15/5/3 (Item 1 from file: 347)

DIALOG(R) File 347:JAPIO

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03453079

BRIGHTNESS INTERPOLATION TYPE WAVEFORM DISPLAY DEVICE

PUB. NO.: 03-115979 [JP 3115979 A]

PUBLISHED: May 16, 1991 (19910516)

INVENTOR(s): SENBA MASATO

APPLICANT(s): NIPPON KODEN CORP [352274] (A Japanese Company or Corporation), JP (Japan)

APPL. NO.: 01-254973 [JP 89254973]

FILED: September 29, 1989 (19890929)

INTL CLASS: [5] G01R-013/20; G09G-005/36

JAPIO CLASS: 46.1 (INSTRUMENTATION -- Measurement); 44.9 (COMMUNICATION -- Other)

JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessors)

JOURNAL: Section: P, Section No. 1238, Vol. 15, No. 320, Pg. 73, August 15, 1991 (19910815)

ABSTRACT

PURPOSE: To obtain the waveform display device of simple constitution which performs linear brightness interpolation between sampled amplitude data by providing a memory where the amplitude data are stored by sampling an input signal, a serial dot data circuit which performs interpolation between the data, its peripheral auxiliary circuit, etc.

CONSTITUTION: The input waveform amplitude is sampled by a circuit 11 and stored in the SRAM 12. Latch circuits 13 and 13a read the stored data *****out***** in *****sequence***** and hold them, and also generate serial dot data for the brightness interpolation with counters 14 and 14a and a flip-flop 15 and supply them to a *****DRAM***** 16. A memory control

circuit 17 sets the upper area 16U of the *****DRAM***** 16 in read mode and the lower side 16D in write mode respectively and while the former is read to make a waveform display by raster scanning, the serial dot data are written in amplitude *****addresses***** of the latter. After the writing is carried on up to an intermediate *****address*****, the stored data are read out of the SRAM 12 and the reverse operation to said operation is started.

File 2:INSPEC 1969-1996/May W1
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File 8:Ei Compendex*Plus(TM) 1970-1996/Jun W3
(c) 1996 Engineering Info. Inc.

File 14:Mechanical Engineering Abs 1973-1996/Jun
(c) 1996 Cambridge Sci Abs

File 233:Microcomputer Abstracts(TM) 81-1996/May
(c) 1996 Information Today, Inc

File 1:ERIC 1966-1996/Apr
(c) format only 1996 Knight-Ridder Info

File 61:LISA(LIBRARY&INFOSCI) 1969-1996/May
(c) 1996 Reed Reference Publishing

File 202:Information Science Abs. 1966-1996/Jan
(c) 1996 IFI/Plenum Data Corp.

File 6:NTIS 64-1996/Jun W4
Comp. & distr. 1996 NTIS, US Dept of Commerce

File 35:Dissertation Abstracts Online 1861-1996/May
(c) 1996 UMI

File 77:Conference Papers Index 1973-1996/May
(c) 1996 Cambridge Sci Abs

File 103:Energy SciTec 1974-1996/Mar B2
(c)format only 1996 Knight-Ridder Info

File 109:Nuclear Sci. Abs. 1948-1976
(c)format only 1995 Knight-Ridder Info

File 108:Aerospace Database 1962-1996/May
(c) 1996 AIAA

File 239:MathSci(R) 1940-1996/Jun
(c) 1996 American Mathematical Society

File 144:Pascal 1973-1996/Apr
(c) 1996 INIST/CNRS

File 434:SciSearch(R) 1974-1996/Apr W3
(c) 1996 Inst for Sci Info

File 7:Social SciSearch(R) 1972-1996/May W2
(c) 1996 Inst for Sci Info

File 49:PAIS INT. 1976-1996/APR
(c) 1996 Public Affairs Information Service

Set	Items	Description
S1	102	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACC- ESS() (MEMORY OR MEMORIES))))
S2	8	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMM- AND? ? OR MEMORY()REQUEST? ?)
S3	2005	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	0	S1 AND S3
S6	6343	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	286	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8

File 2:INSPEC 1969-1996/May W1
(c) 1996 Institution of Electrical Engineers

File 8:EI Compendex*Plus(TM) 1970-1996/Jun W3
(c) 1996 Engineering Info. Inc.

File 14:Mechanical Engineering Abs 1973-1996/Jun
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File 233:Microcomputer Abstracts(TM) 81-1996/May
(c) 1996 Information Today, Inc

File 1:ERIC 1966-1996/Apr
(c) format only 1996 Knight-Ridder Info

File 61:LISA(LIBRARY&INFOSCI) 1969-1996/May
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(c) 1996 IFI/Plenum Data Corp.

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Comp. & distr. 1996 NTIS, US Dept of Commerce

File 35:Dissertation Abstracts Online 1861-1996/May
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File 77:Conference Papers Index 1973-1996/May
(c) 1996 Cambridge Sci Abs

File 103:Energy SciTec 1974-1996/Mar B2
(c)format only 1996 Knight-Ridder Info.

File 109:Nuclear Sci. Abs. 1948-1976
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File 108:Aerospace Database 1962-1996/May
(c) 1996 AIAA

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File 434:SciSearch(R) 1974-1996/Apr W3
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File 7:Social SciSearch(R) 1972-1996/May W2
(c) 1996 Inst for Sci Info

File 49:PAIS INT. 1976-1996/APR
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Set	Items	Description
S1	102	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORIES))))
S2	8	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S3	2005	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	0	S1 AND S3
S6	6343	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	286	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8
S10	9467	DRAM OR (DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORIES)))
S11	0	S2 AND S10
S12	0	S3 AND S10
S13	4	S6 AND S10
S14	4	RD S13 (unique items)

DIALOG(R)File 8: Ei Compendex*Plus(TM)
(c) 1996 Engineering Info. Inc. All rts. reserv.

04329427 E.I. No: EIP95112923765

Title: Streamlined custom processors: when stock performance won't cut it

Author: Levy, Markus

Source: EDN v 40 n 21 Oct 12 1995. 9pp

Publication Year: 1995

CODEN: EDNSBH ISSN: 0012-7515

Language: English

Document Type: JA; (Journal Article) Treatment: G; (General Review)

Journal Announcement: 9603W3

Abstract: Developing a custom processor is no mean feat but one can rely on several companies for help. To begin, one has to *****sort***** through a wide variety of cores and peripherals. After that comes the difficult task of connecting all the pieces. One can consider this step from the electrical-interface or from the design methodology angle, analyzing approaches vendors have developed and maximizing the system on a chip's performance. One must examine the interfaces that connect the cores to the peripherals, coprocessors, memory, and computational units that become part of the CPU itself. Next, one must consider emulator and hardware-debugging support for cores. It must be noted that most of the pieces or modules are reusable and can be interchanged among the designs. Also, integrating systems functions onto one piece of silicon helps to maintain the design's confidentiality.

Descriptors: Microcomputers; Computer peripheral equipment; Interfaces (computer); Random access storage; LSI circuits; Logic design; Reduced *****instruction***** set computing; Computer hardware description languages; Pipeline processing systems; ROM

Identifiers: Streamlined custom processors; Parameterized modules; Central processing unit; Computational bolt on interface; *****Dynamic*****
*****random***** *****access***** *****memory*****

Classification Codes:

723.1.1 (Computer Programming Languages)

722.4 (Digital Computers & Systems); 722.2 (Computer Peripheral Equipment); 722.1 (Data Storage, Equipment & Techniques); 714.2 (Semiconductor Devices & Integrated Circuits); 721.2 (Logic Elements);

723.1 (Computer Programming)

722 (Computer Hardware); 714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 723 (Computer Software)

72 (COMPUTERS & DATA PROCESSING); 71 (ELECTRONICS & COMMUNICATIONS)

14/5/2 (Item 1 from file: 239)

DIALOG(R)File 239:MathSci(R)

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02936376 CR 87090715

The 68000 microprocessor: architecture, software, and interfacing techniques.

Triebel, Walter A.

Singh, Avtar

Publ: Prentice-Hall, Inc., Englewood Cliffs, NJ

1986, 366 pp. ISBN: 0-13-811357-2

Price: \$34.95

Language: English

Document Type: Book

Journal Announcement: 2809

Subfile: CR (Computing Reviews) ACM

Abstract Length: long (99 lines)

This book is a study of the architecture, software, and interfacing techniques of one of the more widely used 16-bit microprocessors, the Motorola 68000. After a short introduction to microprocessors and microcomputers, the electrical interfaces and internal architecture of the 68000 are briefly surveyed in Chapter 2. This concise chapter may discourage the reader; for instance, the discussion of the internal operation of the 68000 requires adequate knowledge of microprogramming techniques. However, most of the topics considered in this chapter are covered in greater detail later in the book.

Chapters 3 and 4 are devoted to the 68000 microprocessor programming. The first part of Chapter 3 contains a detailed description of the 68000 operand addressing modes. The text is integrated by many clear figures. The *****instruction***** set is then examined. The *****instructions***** are divided into functional groups, certain of which (data movement, integer arithmetic, decimal arithmetic, logic, and shift and rotate *****instructions*****) are considered in this chapter. The discussion continues in Chapter 4, where other groups are analyzed: compare and test, jump and branch, subroutine control, and bit manipulation *****instructions*****. For each group, certain significant *****instructions***** are illustrated in detail. The analysis tends to be lengthy and too detailed even for the novice programmer. It concentrates on the actions occurring as a consequence of the execution of each *****instruction*****. Little attention is given to important issues concerning effective *****instruction***** usage such as *****instruction***** performance and code generation and optimization. A number of examples of assembly programs are included, with a difficulty level ranging from elementary problems, such as adding two long words, to more complex problems, such as BCD to binary number conversion and array *****sorting*****. Important issues concerning the operation of an assembler program are also briefly considered.

Chapter 5 deals with the utilization of the MC68000 educational microcomputer. This is a simplified program development system that includes, in addition to the 68000 microprocessor, a 16 Kbyte read-only memory for the storage of a monitor program called the\it Tutor monitor\rm , a 64 Kbyte read-write memory for the storage of user programs and data, parallel I/O ports, and RS-232C serial ports. First, the user interface of the monitor program is illustrated. Its *****commands***** are analyzed in groups: register display/modify *****commands***** , memory display/modify/search *****commands***** , and *****commands***** for control of I/O resources. The process of assembling, executing, and debugging a program is then considered. Sample Tutor sessions are shown, with particular attention to the utilization of tracing and breakpoint techniques. This chapter is of little interest for a reader not involved in the utilization of the educational microcomputer. The level of detail in the analysis of the *****command***** set is excessive, and the possible audience of the material presented seems too narrow for an entire chapter.

Chapters 6--8 cover hardware issues concerning the interfacing of the 68000 microprocessor. Chapter 6 studies the memory and I/O interfaces. Memory cycle timings are illustrated, and an example of a *****dynamic***** *****RAM***** subsystem is presented. The 6821 peripheral interface adapter is examined and used to implement two 16-bit ports for a 68000 microcomputer system. Serial communications are then considered, and the utilization of the 6850 asynchronous communications interface adapter in the construction of an asynchronous serial data communication interface is discussed. The chapter concludes with an analysis of the 68230 parallel interface/timer. In this case, too, examples of applications are examined. This chapter cannot be used as a substitute for a careful reading of the data sheets (the 68230 data sheet is reproduced at the end of the book), but can be taken as a useful complement.

Chapter 7 deals with exception processing of the 68000. The different

methods for initiating an exception are detailed, and the 68000 external hardware interrupt interface is discussed.

Finally, Chapter 8 presents the hardware of the MC68000 educational microcomputer board. In fact, this chapter basically discusses the implementation of a simple 68000-based microcomputer system.

Each chapter includes an assignment section in which certain problems are presented. Answers are given at the end of the book. The Bibliography is not adequate; although several references to works on the 68000 are included, there is poor coverage of important issues likely to be of interest to the reader, e.g., *****instruction***** set organization, assembly language programming, microprocessor interfacing, and microprogramming techniques. The book does include a comprehensive Index.

In conclusion, I feel that this book could be used with profit as a study case in an undergraduate course on computer architecture. Software issues are approached at an elementary level, which is suitable for the novice programmer with little or no knowledge of assembly languages and programming techniques. However, understanding of the hardware issues would require an adequate background in integrated digital electronics, microprocessor interfacing, and microprocessor system design.

Reviewer: L. Lopriore Pisa, Italy

Review Type: Signed Review

Descriptors: *C.5.3 -Computer Systems Organization-COMPUTER SYSTEM IMPLEMENTATION-Microcomputers-Motorola 68000 ; B.7.1 -Hardware-INTEGRATED CIRCUITS-Types and Design Styles-Microprocessors and microcomputers

Identifiers: DESIGN

14/5/3 (Item 2 from file: 239)

DIALOG(R) File 239:MathSci(R)

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02867753 CR 86110979

Computer organization: hardware/software (2nd ed.).

Gorsline, George W. (Virginia Polytechnic Institute and State Univ., Blacksburg,

Publ: Prentice-Hall, Inc., Englewood Cliffs, NJ

1986, 616 pp. ISBN: 0-13-165325-3

Price: \$40.95

Language: English

Document Type: Book

Journal Announcement: 2711

Subfile: CR (Computing Reviews) ACM

Abstract Length: long (91 lines)

This book is essentially two volumes in one. The first five-and-a-half chapters are intended for a 'late-sophomore, early-junior year course' in computer architecture for students with a computer science (as opposed to engineering) background. The remaining three-and-a-half chapters are intended as the focus for a 'dual-level course designed for a mixture of beginning graduate students and seniors with a grounding in circuits, assemblers, languages, and operating systems.' If there is a hierarchy from 'computer systems' to 'computer architecture' to 'computer organization' to 'logic design,' this book would fall somewhere within the top two levels. Despite the subtitle ('Hardware/Software'), coverage of software topics is minimal.

Chapter 1, The Basics, covers data types, direct addressing, and registers. Chapter 2, *****Instructions***** and Modalities, deals with operation codes, addressing modes, and *****instruction***** sets. Chapter 3, The Control Unit, introduces *****instruction***** processing with a discussion of microprogrammings and some examples of CPU organization. Chapter 4, Memories, includes material ranging from cache to virtual

memory, such as core and solid-state memory implementations, pseudodisks, and purchase of add-on primary memory, among other topics. Chapter 5, Input/Output, Data Paths, and Interrupts, surveys various I/O systems and includes material on bus structures and types of I/O devices. Chapter 6, The von Neumann SISD Computer, discusses single processor concurrency, IBM, DEC and Intel families of processors, language directed machines, and the Reduced *****Instruction***** Set Computer (RISC) concept. Chapter 7, Multiprocessors and Multicomputers: MIMD Systems, uses the IBM/370AP and 308X, the Intel 432, C.mmp, and CM* as its examples. Chapter 8, Special Purpose Systems, covers array and vector processors (FPS, Cray), SIMD machines (Illiac IV, BSP, Staran, and MPP), data driven processors (data flow and reduction), and the database machine concept. Chapter 9, Computer Networks, includes network topologies, the ISO model, channel implementations, and examples including Bisync, SNA, DECNET, and Ethernet.

The material is somewhat expanded and *****reordered***** compared to the first edition [1]. New material includes descriptions of several I/O devices in Chapter 5 and descriptions of newer processors (VAX, I8086 family, Cray, FPS, Cyber 205, IBM 370AP and 308X) in various places.

The two best features of the book are (1) its wealth of material covered, and (2) its high degree of accuracy in presenting the material. There are exceptions to both of these assets, of course. For example, intermessage processors (IMPs) are mentioned throughout the networking chapter, but ARPANET (to say nothing of CSNET, BITNET, etc.) is never mentioned at all. Workstations, graphics processors, and other ``special purpose systems,`` such as systolic arrays, the Ultracomputer, the Hypercube, and the Non-Von systems are also conspicuous by their absence. The inaccuracies of which I am aware seem fairly minor. Examples include a garbled description of the use of autoincrement addressing with memory-mapped I/O (p. 222); the suggestion that dynamic memory (*****DRAM*****) refreshing is typically an operating system function (p. 198); nonstandard definitions of software process states (p. 239); and a definition of ``sequential machines`` in terms of *****instruction***** addressing (p. 110).

The major problem with the book is poor organization, and this problem exists at numerous levels. Starting with the Table of Contents one sees little rationale evident for the choice of material to be included in the chapters and little evidence of logical development of topics within each chapter. The typographical layout of the headings within the chapters does not always provide structural guides to the reader, and capitalization of terms within the text is inconsistent. Terms are regularly used before being defined, and terminology is inconsistent (p. 213 compares write-through with write-out algorithms, but p. 326 compares write-through with write-back, for example). Bell and Newell's Processor/Memory/Switch (PMS) notation [2] is introduced early in Chapter 1, then used only infrequently throughout the volume, and finally another (equivalent) notation is introduced in the last chapter for network topologies. Coverage is necessarily shallow for a book which intends to cover so much material in a one-semester course, but the poor organization makes the coverage seem uneven as well. Each chapter ends with some mixture of ``problems,`` ``investigations,`` and ``projects.`` While these exercises are also uneven in quality, there are several excellent ones an instructor could use as models for homework assignments.

The book could be used as an excellent secondary reference by students of the field. The Index is good, and the ten-page Bibliography (which contains references as late as early 1985) is well-referenced within the text.

Reviewer: C. Vickery Flushing, NY

Review Type: Signed Review

Cited References: [1] GORSLINE, G. W. Computer organization: hardware/software, Prentice-Hall, Englewood Cliffs, NJ, 1980. See CR21, 9

(Sept. 1980), Rev. 36,739. [2]BELL, C. G.; AND NEWELL, A. Computer structures: readings and examples, McGraw-Hill, New York, 1971. SeeCR12, 5 (May 1971), Rev. 21,279.

Descriptors: *C.0 -Computer Systems Organization-GENERAL ; B.0 -Hardware-GENERAL; C.2.0 -Computer Systems Organization-COMPUTER-COMMUNICATION NETWORKS-General; D.0 -Software-GENERAL

Identifiers: DESIGN PERFORMANCE

14/5/4 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
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00416699 PASCAL No.: 74-0004075

A 4K MOS *****DYNAMIC***** *****RANDOM*****-*****ACCESS*****

*****MEMORY*****

ABBOTT R A; REGITZ W M; KARP J A

INTEL CORP., SANTA CLARA,CALIF. 95051

Journal: I.E.E.E. J. SOLID-STATE CIRCUITS, 1973, 8 (5) 292-298

Availability: CNRS-222L

No. of Refs.: 18 REF.

Document Type: P (SERIAL) ; A (ANALYTIC)

Country of Publication: USA

Language: ENGLISH

LE COUT DES COMPOSANTS DE CETTE MEMOIRE EST MINIMALISE PAR LA REDUCTION MAXIMALE DU COUT DE LA PASTILLE; CECI EST REALISE PAR L'EMPLOI DE PETITES DIMENSIONS DE PASTILLE AVEC UNE DENSITE DE MEMOIRE ELEVEE (3 DISPOSITIFS PAR CELLULE; TECHNOLOGIE DE L'ELECTRODE DE *****COMMANDE***** AU SILICIUM AVEC CANAL DE TYPE N). LA PASTILLE NECESSITE SEULEMENT UNE BASE DE TEMPS MONOPHASEE ET GENERE DE FACON INTERNE LA SYNCHRONISATION SUR PLUSIEURS PHASES. MISE A PART LA BASE DE TEMPS, TOUTES LES ENTREES ET LA *****SORTIE***** SONT EN CIRCUITS DE LOGIQUE "TOUT TRANSISTOR" COMPATIBLES. (CNET)

English Descriptors: TRANSISTOR TRANSISTOR LOGIC; MEMORY; RANDOM ACCESS MEMORY(RAM); DYNAMICAL STORAGE; MOS TECHNOLOGY

English Generic Descriptors: ELECTRONICS

French Descriptors: MEMOIRE ACCES DIRECT; MEMOIRE DYNAMIQUE; MEMOIRE CYCLIQUE; TECHNOLOGIE MOS; MEMOIRE; LOGIQUE TRANSISTOR TRANSISTOR; LOGIQUE COMPATIBLE; TECHNOLOGIE

French Generic Descriptors: ELECTRONIQUE

Classification Codes: 145A04E03

File 2:INSPEC 1969-1996/May W1
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File 8:Ei Compendex*Plus(TM) 1970-1996/Jun W3
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(c) 1996 Cambridge Sci Abs
File 233:Microcomputer Abstracts(TM) 81-1996/May
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File 1:ERIC 1966-1996/Apr
(c) format only 1996 Knight-Ridder Info
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Comp. & distr. 1996 NTIS, US Dept of Commerce
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(c) 1996 UMI
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(c) 1996 Cambridge Sci Abs
File 103:Energy SciTec 1974-1996/Mar B2
(c)format only 1996 Knight-Ridder Info
File 109:Nuclear Sci. Abs. 1948-1976
(c)format only 1995 Knight-Ridder Info
File 108:Aerospace Database 1962-1996/May
(c) 1996 AIAA
File 239:MathSci(R) 1940-1996/Jun
(c) 1996 American Mathematical Society
File 144:Pascal 1973-1996/Apr
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(c) 1996 Inst for Sci Info
File 7:Social SciSearch(R) 1972-1996/May W2
(c) 1996 Inst for Sci Info
File 49:PAIS INT. 1976-1996/APR
(c) 1996 Public Affairs Information Service

Set	Items	Description
S1	102	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORIES))))
S2	8	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S3	2005	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	0	S1 AND S3
S6	6343	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR COMMAND? ? OR MEMORY()REQUEST? ?)
S7	0	S1 AND S6
S8	286	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	0	S1 AND S8
S10	9467	DRAM OR (DYNAMIC() (RAM OR RANDOM() ACCESS() (MEMORY OR MEMORIES)))
S11	0	S2 AND S10
S12	0	S3 AND S10
S13	4	S6 AND S10
S14	4	RD S13 (unique items)
S15	0	S8 AND S10
S16	67853	RAM OR (RANDOM() ACCESS() (MEMORY OR MEMORIES))

S17 15 S3 AND S16
S18 15 RD S17 (unique items)

18/5/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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02937229 INSPEC Abstract Number: C87048703

Title: GW-BASIC with DOS convenience

Author(s): Lukas-Simonyi, H.

Journal: Mikrocomputer Zeitschrift no.5 p.106-7

Publication Date: May 1987 Country of Publication: West Germany

CODEN: MDMZDL ISSN: 0720-4442

Language: German Document Type: Journal Paper (JP)

Treatment: Practical (P)

Abstract: The GW-BASIC program SHELLBAS which enables the frequently arising requirement of diskette data content reorganisation to be met, is introduced. The program generates a sorted directory, and provides procedures for selectable options of erase, copy, rename, *****sort*****, and Wordstar/ASCII file conversion. All MS-DOS *****instructions***** can be executed from BASIC by means of the Shell instruction. The BASIC Program listing is given and the routines are described. (0 Refs)

Descriptors: BASIC listings; utility programs

Identifiers: *****RAM*****-disk; GW-BASIC program; SHELLBAS; diskette data content reorganisation; sorted directory; erase; copy; rename; sort; Wordstar/ASCII file conversion; Shell instruction

Class Codes: C6150E (General utility programs)

18/5/2 (Item 1 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0339453 94WN02-007

Q&A 4.0: database arrives in Windows

Gartner, John

Windows Magazine , February 1, 1994 , v5 n2 p124-126, 2 Page(s) ISSN: 1060-1066

Company Name: Symantec

Product Name: Q&A

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): B

Hardware/Software Compatibility: IBM PC Compatible; Microsoft Windows

Geographic Location: United States

Presents a favorable review of Q&A v4.0 (\$249), a combination word processor and flat-file database, from Symantec Corp. (800, 408). Runs on IBM PC compatibles with 4MB RAM, 9MB free hard disk space, and Windows. Claims that creating a database is easy with Q&A, and users do not need to learn programming or database syntax to produce effective applications. Notes that Q&A supports all popular data formats, and data can be edited in screen form, or using a spreadsheet view. Praises the program's intelligent assistant, DAVE (Do Anything Very Easily), which provides English-language commands for querying, sorting, and producing custom reports and scripts. Also reports that Q&A offers context-sensitive help and well-written documentation, along with numerous advanced programming and customization options. However, says the program lacks polish, and database performance is slow during queries and sorts. Includes one screen display. (jo)

Descriptors: Database; Word Processing; Window Software; Software Review; Structured Query Language; Report Generator

Identifiers: Q&A; Symantec

18/5/3 (Item 2 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0246398 91IW08-146

AskSam 5.0 adds databaselike relationality Package continues to split functionality between text retrieval and database chores.

Marshall, Patrick

InfoWorld , August 12, 1991 , v13 n32 p67-71, 3 Pages ISSN: 0199-6649

Company Name: AskSam Systems

Product Name: AskSam

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): C

Hardware/Software Compatibility: IBM PC; IBM PC Compatible

Geographic Location: United States

Presents a mixed review of AskSam v. 5.0 (\$395; developer's version including one runtime version, \$695), text-retrieval software that is the most databaselike of its competition from AskSam Systems of Perry, FL (800). Requires IBM PC AT, PS/2, or compatible with 384K of RAM, DOS 2.0 or later, and a hard drive recommended. Says that the upgrade includes new relational retrieval capabilities and application-building commands, it supports optional data fields and record sorting, data importing is fast and easy, and it can retrieve graphics files, but most users will find the advanced features too difficult to learn and use, documentation is not very helpful, and learning the program requires repeated rereading and calls to technical support. Rated 5.2 overall. Includes one screen display, a table of benchmark test results comparing four programs, ratings in 11 categories, and a product summary. (jb)

Descriptors: Information Retrieval; Database; Text; Software Review

Identifiers: AskSam; AskSam Systems

18/5/4 (Item 3 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0216783 90PW05-021

Turbo Basic compiler reborn as PowerBASIC

Spector, Lincoln

PC World , May 1, 1990 , v8 n5 p96, 1 Pages ISSN: 0737-8939

Languages: English

Document Type: Product Announcement

Geographic Location: United States

Announces PowerBASIC 2.0 (\$109.95), a programming language from Spectra Publishing, Sunnyvale, CA (408). The language is an upgrade of Borland's Turbo Basic, and now includes fixed and floating-point BCD formats, has a new procedural math option for systems without a coprocessor which produces faster, but larger, programs. String space, which was formerly restricted to 64K, can now use all available memory, and commands have been added for sorting, scanning, adding, and removing elements of an array. The package now includes a debugger with single step, break point, watch variables, and immediate evaluation and modification. The program requires 640K RAM and DOS 2.0 or later. Includes one screen display. (djd)

Descriptors: Basic; Compiler; Programming Language

Identifiers: PowerBASIC; Spectra Publishing

18/5/5 (Item 4 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0216049 90PX05-037

Client Manager Not just another database

Roddy, Ellen Louise

PCM , May 1, 1990 , v8 n11 p111-112, 2 Pages ISSN: 0747-0460

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): B

Hardware/Software Compatibility: IBM PC; IBM PC Compatible; Tandy;
Microsoft Word; WordPerfect; Wordstar 2000

Geographic Location: United States

Presents a favorable review of Client Manager (\$69.95), a database manager from SimplSoft Products, Inc. of Boulder, CO (303). Requires 256K RAM, DOS 2.11 or later, at least one disk drive and a printer. States the menus are clear and easy to understand, notes can be added to records, provides a command for field duplication, date fields can be sorted, and report forms can be created or preexisting ones can be modified. Includes every label format and provides support for Word, WordPerfect, and Wordstar 2000 in mail merge function. Says Client Manager is the great equalizer.
(vl)

Descriptors: Data Base Management; Database; Software Review

Identifiers: Client Manager; SimplSoft Products

18/5/6 (Item 5 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0194251 89HC06-022

Dinosaurs

Holzberg, Carol S

Home Office Computing , June 1, 1989 , v7 n6 p86, 1 Pages ISSN:
0899-7373

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): b

Hardware/Software Compatibility: IBM PC Compatible; Commodore 64;
Apple; IBM PS/2 Compatible

Geographic Location: United States

Presents a favorable review of Dinosaurs (\$35-\$40), an educational program for children ages 2-5 from Advanced Ideas Inc., Berkeley, CA (415). The program requires a 64K Apple, Commodore 64, or IBM PC, PS/2 or compatible with 256K RAM. It contains five games which teach sorting, counting, and reading skills. The instruction is picture oriented, so children can begin to play immediately, and the documentation contains descriptions of the dinosaurs featured in the program, six pages for coloring, and suggestions for off-line activities. (djd)

Descriptors: Education; Software Review

Identifiers: Dinosaurs; Advanced Ideas

18/5/7 (Item 6 from file: 233)
DIALOG(R)File 233:Microcomputer Abstracts(TM)
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0182472 88MW12-008

HyperTools #1 and HyperTools #2

Stefanac, Suzanne

Macworld , December 1, 1988 , v5 n12 p160-162, 2 Pages ISSN: 0741-8647

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): B; B

Hardware/Software Compatibility: Macintosh

Geographic Location: United States

Presents favorable reviews of HyperTools #1 and HyperTools #2 (\$99.95 each), two HyperCard tool kits from Softworks of Huntington, CT (203). Runs on a Macintosh with 1MB RAM and HyperCard 1.2. Says the 16 tools in each package are powerful and facilitate many HyperCard authoring routines but that it is imperative to follow the manual's instructions when using the tools, especially the Reorder tool. Includes two screen displays. (jb)

Descriptors: HyperCard; Software Tools; Kit; Software Review

Identifiers: HyperTools #1; HyperTools #2; Softworks

18/5/8 (Item 7 from file: 233)

DIALOG(R)File 233:Microcomputer Abstracts(TM)

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0143319 87PW05-011

WindowDOS: RAM-resident hard disk manager

Marshall, Patrick

PC World , May 1987 , v5 n5 p150-152, 2 Pages ISSN: 0737-8939

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): A

Geographic Location: United States

Presents a very favorable review of WindowDOS version 2.0 (\$49.95), a memory resident hard disk manager from WindowDOS Associates of Arlington, TX (817). WindowDOS requires 40K, one disk drive, and DOS 2.00 or later. WindowDOS offers many options such as changing the default drive or directory, checking the free space on any drive, sorting files in any order chosen, etc. The pop-up menu has eleven "command switches" listed at the bottom of the menu. The primary advantage of using WindowDOS is that there is no need to exit the program even if renaming subdirectories. The complaints were about the "tree-style directory" and "text-file display" because they were not considered as good as XTree's. Contains one screen display.

Descriptors: DATA BASE MANAGEMENT; DISK FILES; SOFTWARE REVIEW

Identifiers: WindowDOS; WindowDOS Associates

18/5/9 (Item 8 from file: 233)

DIALOG(R)File 233:Microcomputer Abstracts(TM)

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0137276 87IC02-010

A database discovery

Grevstad, Eric

inCider , Feb 1987 , v5 n2 p97-99, 3 Pages ISSN: 0740-0101

Languages: English

Document Type: Software Review

Grade (of Product Reviewed): B

Hardware/Software Compatibility: Apple IIe; Apple IIC; Apple IIGS

Geographic Location: United States

Presents a favorable review of Nite Owl Journal #1 (\$29.95), a home database manager from Nite Owl Productions of Mission, KS. Notes that it

requires 64K RAM to run on an Apple IIe, IIc, or IIGS. Discusses its user interface, editing commands, sorting features, and reporting capabilities. Says that it is fast and easy to use and comes with a good disk-copying utility. (b1)

Descriptors: DATA BASE MANAGEMENT; SOFTWARE REVIEW; HOME

Identifiers: Nite Owl Journal #1; Nite Owl Productions

18/5/10 (Item 9 from file: 233)

DIALOG(R) File 233:Microcomputer Abstracts(TM)

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0133543 86MI12-003

SORT-AID: A Search Post-Processing Tool Set

Leigh, William; Paz, Noemi; Vital, Dennis; Huffman, G David

Microcomputers for Information Management , Dec 1986 , v3 n4 p281-295,

15 Pages ISSN: 0742-2342

Languages: English

Document Type: Article

Geographic Location: United States

Describes a collection of computer programs called SORT-AID which were designed by the authors to allow online searchers to organize, review, and analyze citations that have been downloaded from a bibliographic database. Notes that it requires 512K RAM and an IBM PC. Says that it provides a quick, free-text searching capability, allows the user to rank records by their relevance, and is inexpensive to install and use. Provides an example of a search session using SORT-AID. States that searchers have been enthusiastic about using the program. Includes a dictionary of program commands. Includes five references, one flow chart of the SORT-AID system, and four screen displays.

Descriptors: INFORMATION RETRIEVAL; ONLINE INFORMATION; SORTING; SOFTWARE EVALUATION

Identifiers: SORT-AID

18/5/11 (Item 1 from file: 144)

DIALOG(R) File 144:Pascal

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10417490 PASCAL No.: 92-0620968

On-chip test circuitry for a 2-ns cycle, 512-kb CMOS ECL SRAM

SCHUSTER S E; CHAPPELL T I; CHAPPELL B A; FRANCH R L

IBM Thomas J. Watson res. cent., Yorktown Heights NY 10598, USA

Journal: IEEE journal of solid-state circuits, 1992, 27 (7) 1073-1079

ISSN: 0018-9200 CODEN: IJSCBC Availability: INIST-222 L;

354000028943360160

No. of Refs.: 5 ref.

Document Type: P (Serial) ; A (Analytic)

Country of Publication: USA

Language: English

On-chip test circuitry that provides 8-b-deep ECL-level patterns to 12 input pads of a 512-kb CMOS ECL SRAM at cycle times as fast as 1.4 ns has been built in a 0.8- μ m CMOS technology with $L_{SUB e SUB f SUB f} = 0.5 \mu$ m. A unique approach for synchronizing the input signals to the chip-select signal in order to provide optimum setup time and data-valid window as the operating frequency changes is described. Measured results and extensive simulation demonstrate the stability of the on-chip test circuitry for cycle times of 1.4-50 ns. The on-chip test circuitry makes it possible to test the SRAM chip at its pipelined cycle time

English Descriptors: *****Random***** *****access***** *****memory***** (

*****RAM*****); Static storage; Emitter coupled logic; Complementary MOS technology; Simulation; Test; Digital circuit; Monolithic integrated circuit; Operation study; Voltage controlled oscillator; Stability; Waveform; Synchronization; Output circuit; Electrical characteristic

French Descriptors: Memoire acces direct; Memoire statique; Logique emetteur couple; Technologie MOS complementaire; Simulation; Essai; Circuit numerique; Circuit integre monolithique; Analyse fonctionnement; Oscillateur *****commande***** tension; Stabilite; Forme onde; Synchronisation; Circuit *****sortie*****; Caracteristique electrique

Classification Codes: 001D03F06B

18/5/12 (Item 2 from file: 144)
DIALOG(R) File 144:Pascal
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06138432 PASCAL No.: 85-0400182
Lower bounds for *****sorting***** with realistic *****instruction***** sets
DITTE E; O'DONNELL M J
New Mexico state univ., dep. computer sci., Los Cruces NM 88003, USA
Journal: IEEE transactions on computers, 1985, 34 (4) 311-317
ISSN: 0018-9340 Availability: CNRS-222F4
No. of Refs.: 12 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: USA
Language: English
On montre qu'un temps OMEGA ($n \log n$) est necessaire pour trier n entiers a l'aide de comparaisons, additions, soustractions, multiplications, divisions, adressage indirect et troncation restreinte

English Descriptors: Computing complexity; Sorting; Inferior bound; Interpolation; Decision tree; *****Random***** *****access*****
*****memory***** (*****RAM*****)

French Descriptors: Complexite calcul; Triage; Limite inferieure; Interpolation; Arbre decision; Memoire acces direct

Classification Codes: 001D02A05

18/5/13 (Item 3 from file: 144)
DIALOG(R) File 144:Pascal
(c) 1996 INIST/CNRS. All rts. reserv.

05336885 PASCAL No.: 85-0036891
Circuit techniques for a 25 ns 16K X1 SRAM using address-transition detection
BARNES J J; DE JESUS A L; NOVOSEL D
MOS IC group, Austin TX 78721, USA
Journal: IEEE journal of solid-state circuits, 1984, 19 (4) 455-461
ISSN: 0018-9200 Availability: CNRS-222L
No. of Refs.: 8 ref.
Document Type: P (Serial) ; A (Analytic)
Country of Publication: USA
Language: English
L'utilisation du circuit de detection de transitions d'adresses pour

reduire la puissance et ameliorer la vitesse des memoires statiques est admise. Description d'un circuit special donnant une memoire statique a acces direct a 16 K en technologie HMOS. Etude d'un nouveau circuit de *****commande***** de *****sortie***** de decodeur de lignes et de colonnes

English Descriptors: Memory; *****Random***** *****access*****
*****memory***** (*****RAM*****); Static storage; HMOS technology;
Detection; Transition
French Descriptors: Memoire; Memoire acces direct; Memoire statique;
Technologie HMOS; Detection; Transition; Adresse

Classification Codes: 001D03I02

18/5/14 (Item 4 from file: 144)
DIALOG(R) File 144:Pascal
(c) 1996 INIST/CNRS. All rts. reserv.

03929288 PASCAL No.: 75-0104358
ETUDE ET REALISATIONS D'UN DISPOSITIF FIFO A L'AIDE DES MEMOIRES
*****RAM*****).
SHENTON G
AMI MICROSYSTEMS LTD.,
Journal: EVOLUTION MICROELECTRON. INDUSTR., 1975 (201) 40-41
Availability: CNRS-8181
Document Type: P (SERIAL) ; A (ANALYTIC)
Country of Publication: FRANCE
Language: FRENCH
L'AUTEUR INDIQUE D'ABORD LA FACON D'ADRESSER UNE MEMOIRE MOS A ACCES
SELECTIF POUR REALISER LA FONCTION FIFO (FIRST IN, FIRST OUT) OU "PREMIER
ENTRE-PREMIER *****SORTI*****". LE FONCTIONNEMENT D'UNE TELLE MEMOIRE
COMPREND LA *****COMMANDE***** DE DEUX SELECTEURS D'ADRESSAGE ET UNE
SYNCHRONISATION APPROPRIEE DANS LA GENERATION DES SIGNAUX DE LECTURE ET
ECRITURE. UN DISPOSITIF FIFO DE 2000 OCTETS UTILISE DES MEMOIRES DE 1000
ELEMENTS BINAIRES. LA CELLULE DE MEMOIRE EST DYNAMIQUE ET EXIGE D'ETRE
RAFRAICHIE AU MOINS TOUTES LES 1 A 2 MS. LE RAFRAICHISSEMENT CONTINU EST
PREFERABLE. (CNET)

English Descriptors: MEMORY; *****RANDOM***** *****ACCESS*****
*****MEMORY***** (*****RAM*****); MOS TECHNOLOGY
English Generic Descriptors: ELECTRONICS
French Descriptors: MEMOIRE; MEMOIRE ACCES DIRECT; TECHNOLOGIE MOS;
FONCTION FIFO
French Generic Descriptors: ELECTRONIQUE

Classification Codes: 145A06E03

18/5/15 (Item 5 from file: 144)
DIALOG(R) File 144:Pascal
(c) 1996 INIST/CNRS. All rts. reserv.

02593500 PASCAL No.: 80-0335114
PANORAMA DES CARTES D'UNITE CENTRALE A BASE DE MICROPROCESSEURS
GIROD D
Journal: MINIS ET MICROS, 1979, 4 (106) 15-25
Availability: CNRS-16882

Document Type: P (SERIAL) ; A (ANALYTIC)

Country of Publication: FRANCE

Language: FRENCH

ON INTERROGE 80 CONSTRUCTEURS AFIN D'ETABLIR UN TABLEAU REGROUPANT LES
PRINCIPALES CARACTERISTIQUES DES PRODUITS EXISTANTS

English Descriptors: INPUT OUTPUT; COMPUTER EQUIPMENT; INSTRUCTION;
*****RANDOM***** *****ACCESS***** *****MEMORY***** (*****RAM*****); READ
ONLY MEMORY(ROM); MICROPROCESSOR; MINICOMPUTERS; COMPUTER SYSTEM;
TECHNOLOGY; CENTRAL UNIT

English Generic Descriptors: COMPUTER SCIENCES

French Descriptors: MICROPROCESSEUR; UNITE CENTRALE; MINIORDINATEUR;
*****INSTRUCTION*****; TECHNOLOGIE; MEMOIRE ACCES DIRECT; MEMOIRE MORTE;
ENTREE *****SORTIE*****; SYSTEME INFORMATIQUE; EQUIPEMENT INFORMATIQUE;
MONOCARTE; CARTE UNITE CENTRALE

French Generic Descriptors: INFORMATIQUE

Classification Codes: 110C04H05

File 275:IAC(SM) Computer Database(TM) 1983-1996/May 10
 (c) 1996 Info Access Co
 File 148:IAC Trade & Industry Database 1976-1996/May 10
 (c) 1996 Info Access Co
 File 674:Computer News Fulltext 1989-1996/May W1
 (c) 1996 IDG Communications
 File 624:McGraw-Hill Publications 1985-1996/May 09
 (c) 1996 McGraw-Hill Co. Inc
 File 623:Business Week 1985-1996/May W1
 (c) 1996 The McGraw-Hill Companies Inc
 File 746:Time Publications 1985-1996
 (c) 1996 Time Inc.
 File 646:Consumer Reports 1982-1996/Apr.
 (c) 1996 Consumer Union
 File 88:IAC BUSINESS A.R.T.S. 1976-1996/May W1
 (c) 1996 Information Access Co
 File 9:Business & Industry(TM) Jul 1994-1996/May 10
 (c) 1996 Resp. DB Svcs.
 File 12:IAC Industry Express (sm) 1995-1996/May 10
 (c) 1996 Info. Access Co.
 File 636:IAC Newsletter DB(TM) 1987-1996/May 10
 (c) 1996 Information Access Co.
 File 15:ABI/INFORM(R) 1971-1996/May W2
 (c) 1996 UMI
 File 16:IAC PROMT(R) 1972-1996/May 10
 (c) 1996 Information Access Co.
 File 47:Magazine Database(TM) 1959-1996/May 10
 (c) 1996 INFORMATION ACCESS CO.
 File 75:IAC Management Contents(R) 86-1996/May W1
 (c) 1996 Info Access Co

Set	Items	Description
S1	1339	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACC- ESS() (MEMORY OR MEMORIES))))
S2	32	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMM- AND? ? OR MEMORY()REQUEST? ?)
S3	4415	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	8	S1 AND S3
S6	66425	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S7	31	S1 AND S6
S8	1066	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	5	S1 AND S8
S10	6	RD S5 (unique items)

10/3,KWIC/1 (Item 1 from file: 275)
 DIALOG(R) File 275:IAC(SM) Computer Database(TM)
 (c) 1996 Info Access Co. All rts. reserv.

01874195 SUPPLIER NUMBER: 17800526 (USE FORMAT 7 OR 9 FOR FULL TEXT)
 Graphics drive video DRAMs. (graphics memory requirements forces new DRAM
 development) (EE Times 1996 Multimedia Yearbook) (Technology Information)
 Wilson, Ron
 Electronic Engineering Times, n876, p74(5)
 Nov, 1995
 ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
 WORD COUNT: 2496 LINE COUNT: 00186

...ABSTRACT: changing how data memory requests are ordered. New DRAMs, such as Video RAM, Windows RAM, *****SDRAM***** and Rambus DRAMs, are beginning to feature a number of specialized functions that allocate tasks ...

TEXT:
...for faster varieties of DRAMs. Many have abandoned conventional memories for such advanced solutions as *****synchronous*****
*****DRAM***** (*****SDRAM*****) or Rambus DRAM.
... of page misses. On the controller side, multimedia systems designers are trying to buffer and *****reorder***** *****memory*****
*****requests***** to stay on-page for as long as possible.
Memory vendors have been face to...

10/3,KWIC/2 (Item 2 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
(c) 1996 Info Access Co. All rts. reserv.

01874189 SUPPLIER NUMBER: 17800514 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Programmable solution on tap. (Philips Semiconductors' TriMedia VLIW-based processor) (EE Times 1996 Multimedia Yearbook) (Product Information)
Emigh, Aaron
Electronic Engineering Times, n876, p50(4)
Nov, 1995
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1525 LINE COUNT: 00127

...ABSTRACT: single-chip processor uses special instructions to process comprehensive multimedia tasks. The processor relies on
*****synchronous***** *****DRAM***** and time-shared architecture for enhanced data communications between processor units. Some video processing tasks...

... the instruction decoder does. While the instruction-decoding logic can only see ahead a few *****instructions***** , the compiler has access to the entire program and can *****reorder***** *****instructions***** globally as appropriate to maximize parallelism. As compared with a hybrid approach, it is more...

...Philips's TM-1 system consists of the TM-1 microprocessor itself, a block of *****synchronous***** *****DRAM***** (*****SDRAM*****), and a small amount of external circuitry to interface to the incoming and/or outgoing...

...is that the CPU and peripherals are time-shared, and communication between units is through *****SDRAM***** memory. The CPU switches from one task to the next; first it decompresses a video...

10/3,KWIC/3 (Item 1 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1996 Info Access Co. All rts. reserv.

08562315 SUPPLIER NUMBER: 18143534 (USE FORMAT 7 OR 9 FOR FULL TEXT)
1996 ISSCC unveils the latest digital, analog, and communication IC designs. (International Solid State Circuits Conference, integrated circuits)
Bursky, Dave
Electronic Design, v44, n2, p44(3)

Jan 22, 1996

ISSN: 0013-4872

LANGUAGE: English

RECORD TYPE: Fulltext; Abstract

WORD COUNT: 2049

LINE COUNT: 00161

... and one from Samsung Electronics, Yongin-Gun, Korea. A third paper details a 256-Mbit *****synchronous***** *****DRAM***** from NEC. Mitsubishi opted for a wide, 64-bit data bus on its 1-Gbit...

...and is housed in a 196-lead BGA package.

Running from 2 V, Samsung's *****synchronous***** *****DRAM***** is made from 0.16-((micro)meter) CMOS (four polysilicon and four metal levels) and...

...multi-bank design, yielding a 1-Gbyte/s data-transfer bandwidth. NEC's 256-Mbit *****synchronous***** *****DRAM***** takes advantage of a synchronous-mirror-delay circuit that synchronizes internal and external clocks to...high-performance RISC CPUs, one x86-compatible CPU with multimedia enhancements, and a 56-entry *****instruction***** *****reorder***** buffer.

Among the five RISC and lone CISC-compatible CPUs discussed is a 64-bit...

...graphic-acceleration functions, and multimedia support.

HP's designers also will detail the 56-entry *****instruction***** *****reorder***** buffer that they developed for the 64-bit PARISC 8000. The has 850,000 transistors...

10/3,KWIC/4 (Item 2 from file: 148)
DIALOG(R)File 148:IAC Trade & Industry Database
(c) 1996 Info Access Co. All rts. reserv.

07714326 SUPPLIER NUMBER: 16682578 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Gigabit DRAMs, 64-bit CPUs and more at ISSCC. (dynamic random access memory; central processing unit; International Solid State Circuits Conference) (includes related article)

Burksy, Dave

Electronic Design, v43, n4, p61(13)

Feb 20, 1995

ISSN: 0013-4872

LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT; ABSTRACT

WORD COUNT: 9237

LINE COUNT: 00710

... Electronics Inc., Kyungki-Do, Korea, detailed a wave-pipelining scheme employed on a 256-Mbit *****synchronous***** *****DRAM*****. The DRAM was fabricated using 0.3-[[micro]meter] features on a twin-well CMOS ...point, and flag variables. Also incorporated are multiprocessing bus support and carefully controlled memory-access *****reordering*****.

The engine predicts the *****instruction***** flow, and the *****instructions***** are decoded into micro-operations or a series of micro-operations. These micro-operations are...

10/3,KWIC/5 (Item 1 from file: 16)
DIALOG(R)File 16:IAC PROMT(R)
(c) 1996 Information Access Co. All rts. reserv.

05908977

Graphics drive video DRAMs -- New architectures emerge, as frame-buffer designers demand faster access times for animation and imaging
Graphics drive video DRAMs - New architectures emerge

... for faster varieties of DRAMs. Many have abandoned conventional memories for such advanced solutions as *****synchronous*****
*****DRAM***** (*****SDRAM*****) or Rambus DRAM.

It is with horror, then, that designers are discovering an ugly truth
...

... for faster varieties of DRAMs. Many have abandoned conventional memories for such advanced solutions as *****synchronous*****
*****DRAM***** (*****SDRAM*****) or Rambus DRAM.

It is with horror, then, that designers are discovering an ugly truth
...of page misses. On the controller side, multimedia systems designers are trying to buffer and *****reorder***** *****memory***** *****requests*****
to stay on-page for as long as possible.

Memory vendors have been face to...

10/3,KWIC/6 (Item 2 from file: 16)

DIALOG(R)File 16:IAC PROMT(R)

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05908971

Programmable solution on tap -- Tomorrow's multimedia machine demands more
than the DSP, and a VLIW-based single chip might be the answer

... the instruction decoder does. While the instruction-decoding logic can only see ahead a few *****instructions***** , the compiler has access to the entire program and can *****reorder***** *****instructions***** globally as appropriate to maximize parallelism. As compared with a hybrid approach, it is more...

... Philips's TM-1 system consists of the TM-1 microprocessor itself, a block of *****synchronous***** *****DRAM***** (*****SDRAM*****), and a small amount of external circuitry to interface to the incoming and/or outgoing...

... is that the CPU and peripherals are time-shared, and communication between units is through *****SDRAM***** memory. The CPU switches from one task to the next; first it decompresses a video...

File 275:IAC(SM) Computer Database(TM) 1983-1996/May 10
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 File 148:IAC Trade & Industry Database 1976-1996/May 10
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 File 674:Computer News Fulltext 1989-1996/May W1
 (c) 1996 IDG Communications
 File 624:McGraw-Hill Publications 1985-1996/May 09
 (c) 1996 McGraw-Hill Co. Inc
 File 623:Business Week 1985-1996/May W1
 (c) 1996 The McGraw-Hill Companies Inc
 File 746:Time Publications 1985-1996
 (c) 1996 Time Inc.
 File 646:Consumer Reports 1982-1996/Apr.
 (c) 1996 Consumer Union
 File 88:IAC BUSINESS A.R.T.S. 1976-1996/May W1
 (c) 1996 Information Access Co
 File 9:Business & Industry(TM) Jul 1994-1996/May 10
 (c) 1996 Resp. DB Svcs.
 File 12:IAC Industry Express (sm) 1995-1996/May 10
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 File 636:IAC Newsletter DB(TM) 1987-1996/May 10
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 File 15:ABI/INFORM(R) 1971-1996/May W2
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 File 16:IAC PROMT(R) 1972-1996/May 10
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 File 47:Magazine Database(TM) 1959-1996/May 10
 (c) 1996 INFORMATION ACCESS CO.
 File 75:IAC Management Contents(R) 86-1996/May W1
 (c) 1996 Info Access Co

Set	Items	Description
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S4	0	S1 AND S2
S5	8	S1 AND S3
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S7	31	S1 AND S6
S8	1066	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	5	S1 AND S8
S10	6	RD S5 (unique items)
S11	23	S7 NOT S5
S12	15	RD S11 (unique items)

12/3,KWIC/1 (Item 1 from file: 275)
 DIALOG(R) File 275:IAC(SM) Computer Database(TM)
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01927081 SUPPLIER NUMBER: 18181375 (USE FORMAT 7 OR 9 FOR FULL TEXT)
 M'soft sends PC message. (Microsoft demos Simple Interactive PC at Windows
 Hardware Engineering Conference) (Industry Trend or Event)
 Boyd-Merritt, Rick
 Electronic Engineering Times, n896, p1(2)
 April 8, 1996

ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2052 LINE COUNT: 00158

... Gates said in the interview. "Everything we talk about under the SIPC banner is just *****sort***** of the first phase of what we need to do."

Microsoft and Intel Corp. have...

...surround-sound audio;

- * prepare to run MPEG and sound functions on Intel's MMX X86-*****instruction*****-set extensions;
- * prepare to support MPEG-2 and AC-3 for DVD players;
- * plan for 16-Mbyte *****SDRAM***** or SGRAM main memory;
- * keep quality L2 caches in systems to support multimedia and multitasking...

12/3,KWIC/2 (Item 2 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
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01887801 SUPPLIER NUMBER: 17986336 (USE FORMAT 7 OR 9 FOR FULL TEXT)
All work & some play: shopping for a small-office, home-office, or family PC. (Shopper's Guide: Family/SOHO PCs)(includes related articles on laptops, PC/Mac coexistence, shopping tips, and family-oriented software front ends)(Buyers Guide)
Stone, M. David
Computer Shopper, v16, n2, p304(14)
Feb, 1996
DOCUMENT TYPE: Buyers Guide ISSN: 0886-0556 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 6002 LINE COUNT: 00470

... or internal, cache. Cache is critical to performance because the CPU can process data and *****instructions***** held in the cache without waiting for them to arrive from slower system RAM.
Most...

...fast as those that combine ordinary DRAM with cache.

Other fast DRAM technologies such as *****synchronous*****
*****DRAM***** (*****SDRAM*****), which is now found in Toshiba's Pentium-based Tecra notebooks, and burst EDO (BEDO...sales rep edited the file, saved it using the Rich Text Format (RTF) option--a *****sort***** of formatting-friendly step up from plain ASCII text--and returned it to Manley, who...

12/3,KWIC/3 (Item 3 from file: 275)
DIALOG(R)File 275:IAC(SM) Computer Database(TM)
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01866580 SUPPLIER NUMBER: 17707124 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Trade-offs key, as chip sets take center stage. (core logic chip set design)(Special Report: PC Chip Sets)(Technical)
Talraja, Prem
Electronic Engineering Times, n874, p92(2)
Nov 13, 1995
DOCUMENT TYPE: Technical ISSN: 0192-1541 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1439 LINE COUNT: 00115

... disk-drive performance boost-are such that virtually all chip-set vendors now offer some *****sort***** of support for the Bus Master IDE mode.

Integration is an issue in that some...

...flat pack (PQFP) implementations. But while BGAs may offer improvements in motherboard assembly yields, they *****command***** a premium and face supply constraints that have hampered more widespread adoption of BGA packaging...

...bit-wide main memory, UMA can take advantage of the new and faster DRAMs (EDO, *****synchronous***** *****DRAM***** , etc.) while bypassing the 32-bit constraints of the PCI bus. In the long run a non-UMA design that employs *****synchronous***** *****DRAM***** and top-of-the-line 133-MHz processors. But UMA is particularly valuable because it...

12/3,KWIC/4 (Item 4 from file: 275)
DIALOG(R) File 275:IAC(SM) Computer Database(TM)
(c) 1996 Info Access Co. All rts. reserv.

01866574 SUPPLIER NUMBER: 17707112 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Designing computers.(Special Report: PC Chip Sets)(Technical)
Cole, Bernard
Electronic Engineering Times, n874, p75(5)
Nov 13, 1995
DOCUMENT TYPE: Technical ISSN: 0192-1541 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 5160 LINE COUNT: 00402

... in most designs is the memory subsystem.

The time needed to access or fetch an *****instruction***** is largely dependent on the memory system. Memory access time will continue to be the ...

...RISC designs help reduce memory-bandwidth requirements, achieving a completion rate of one or more *****instruction***** per cycle-the rate that has become the norm in most advanced CPU designs-is impossible unless the memory subsystem can deliver the *****instructions***** at the clock rate of the processor. In many of the newer CPUs-almost all...

...address strobe (CAS) cycle-time delay. Burst accesses allow the system logic to provide data/*****instructions***** from memory locations within only the CAS cycle time. The burst throughput can thus be increased and the processor's pipeline and *****instruction***** queues filled sufficiently.

But as memory access time-both row-address strobe (RAS) and column...

...prefetch queue's being flushed. That holds especially true for cases in which the required *****instruction***** extends beyond the first double word of the burst. In such a case, the CPU...

...additional potential performance inhibitors. They have to do with the fact that in the Pentium, *****memory***** *****requests***** come primarily from these sources: direct requests from the execution unit; indirect requests from other...

...requests on behalf of those other functions, indentifying the source, type and length of the *****memory***** *****request***** by a unique set of signals.

Application dictates
The delay and wait states with which...

...For a word processor such as Word operating under Windows 3.1, the number of *****memory***** *****requests***** can be between 4 million and 5 million per second, depending on the kind of...

...one finds that as much as 40 percent of the CPU workload is dominated by *****instruction***** fetches and data writes from the write buffer, with the rest divided ...can push it on the controller side," warned Ng of Oak Technology. "After that, all *****sorts***** of things get in the way: noise, due to the number of pins switching and...

...Via . "The problem now is to find out which of the alternative DRAMs-burst EDO, *****SDRAM***** or, possibly, cache or enhanced DRAM-not only have the necessary bandwidth but also do something to mask the inherent latency of DRAMs."

Hedging bets

As system designers *****sort***** through the alternatives, core-logic vendors are hedging their bets by supporting as many of...

...level caching or find some alternative." Simply going to higher performance DRAM alternatives, such as *****SDRAM***** or burst EDO, will not suffice.

Some of the new UMA core-logic chip sets...by a burst from the system, the CPU doesn't need constant memory access for *****instructions***** and data.

"However, increasing the CPU cache size with relatively more expensive SRAM offsets the...

...rumored to have a second-level cache on board, as well as so-called visual *****instructions***** , similar in function to those proposed by Sun for its Ultrasparc CPU.

Even further ahead...

12/3,KWIC/5 (Item 5 from file: 275)
DIALOG(R) File 275:IAC(SM) Computer Database(TM)
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01824082 SUPPLIER NUMBER: 17187253 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Pentium killers? (AMD's K5, Cyrix's M1, NexGen's Nx586 and Intel's P6 CPUs)
(includes executive summaries) (Hardware Review)(Evaluation)
Kennedy, Randall C.
PC/Computing, v8, n9, p106(9)
Sep, 1995
DOCUMENT TYPE: Evaluation ISSN: 0899-1847 LANGUAGE: English
RECORD TYPE: Fulltext; Abstract
WORD COUNT: 3568 LINE COUNT: 00290

...ABSTRACT: not yet been implemented in systems, but they offer the ability to decode and execute *****instructions***** out of sequence through the use superscalar pipelining. Cyrix's M1 CPU includes support for native x86 *****instructions***** , a feature promises greater speed. The AMD and Cyrix microprocessors offer pin compatibility with Pentiums...
... the cycle all over again. But for now your craving is real, so we've *****sorted***** through the CPU quagmire to make your decision-making easier. We can't completely satisfy...

...looking downright dated, at least from a technological standpoint.

Lacking features like speculative execution, multiple-*****instruction***** execution, and renameable registers, the Pentium may have trouble competing against offerings from AMD and...

...K5 and the M1 feature superscalar, superpipelined designs that speed execution by decoding and executing *****instructions***** in stages. Both use multiple, renameable registers to allow speculative execution and out-of-order...

...avoiding the RISC-core route in favor of optimizing the chip to execute native x86 *****instructions*****. Cyrix claims to have solved the x86 *****instruction***** bottleneck--caused by things such as variable-length *****instructions***** , data dependencies, and limited registers--without resorting to RISC-based emulation. Cyrix also claims to...

...chip, AMD's K5 features a RISC core with on-chip emulation to execute x86 *****instructions*****. However, it differs in how it handles *****instructions***** before executing them; the K5 can pre-decode *****instructions***** as they are placed in its onboard *****instruction***** cache, making them easier to work with as soon as they arrive at the actual...

...performance boost.

The net result is a chip that can issue as many as four *****instructions***** per clock cycle; the Pentium can issue only three. AMD claims that this four-issue...

...M1, and presto--instant turbocharge. And because the processor is strictly compatible with the x86 *****instruction***** set, you don't have to worry about whether you'll be able to run...

...2400

Speed: 100MHz

Price*: \$2,000 to \$4,000

Unique CPU Features: RISC core, four *****instructions***** per clock cycle, branch prediction, Pentium pin compatible, decoder for x86 *****instructions*****.

Processor: M1; Cyrix Corp.; (800) 462-9749, (214) 968-8387

Speed: 100MHz; 120MHz

Price*: \$2,000 to \$2,500

Unique CPU Features: CISC core, two *****instructions***** per clock cycle, branch prediction, Pentium pin-compatible, 16K onboard cache, completely compatible with x86 *****instruction***** set.

Processor: Pentium; Intel Corp.; (800) 548-4725

Speed: 150MHz; 167.7MHz

Price*: \$3,000 to \$4,000

Unique CPU Features: CISC core, two *****instructions***** per clock cycle, branch prediction.

*ESTIMATED STREET PRICES OF FULLY CONFIGURED SYSTEM.

P6: Fast, Cheap...

...75MHz Pentium.

Also, the P6 uses superscalar pipelining, which decouples the decoding part of an *****instruction***** from the execution part (AMD's K5 and NexGen's Nx586 also do this). This allows *****instructions***** to be executed out of order, and it reduces the amount of time the CPU remains idle waiting for the next *****instruction***** to chug down the pipeline--a key to fast server performance.

In addition to the...

...ships, it won't support advanced memory technologies, such as extended data out (EDO) RAM; *****synchronous***** *****dynamic***** *****RAM***** (DRAM), or high-bandwidth Rambus DRAMs. All of these technologies can boost throughput by as...

12/3,KWIC/6 (Item 6 from file: 275)
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01741283 SUPPLIER NUMBER: 16368405 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Philips hopes to displace DSPs with VLIW: TriMedia processors aimed at future multimedia embedded apps. (Philips Electronics TriMedia microprocessor; Digital Signal Processing; Very Long *****Instruction***** Word processors)

Case, Brian

Microprocessor Report, v8, n16, p12(4)

Dec 5, 1994

ISSN: 0899-9341

LANGUAGE: ENGLISH

RECORD TYPE: FULLTEXT

WORD COUNT: 2249

LINE COUNT: 00191

...aimed at future multimedia embedded apps. (Philips Electronics TriMedia microprocessor; Digital Signal Processing; Very Long *****Instruction***** Word processors)

... high performance is parallelism, i.e., multiple operations per cycle. For existing CISC and RISC *****instruction***** sets, this can be achieved only with superscalar implementations. For new *****instruction***** sets, VLIW is the least complex way to achieve superscalar performance (see MPR 2/14...

...are like narrow, specialized VLIWs: they combine two or three independent operations into a single *****instruction*****. For example, a DSP *****instruction***** might perform two separate address calculations, memory accesses, and computations. The data operations and addressing modes of a DSP *****instruction***** set are tailored to the peculiarities of the intended application domain - signal processing algorithms. Some...

...a big hardware advantage over superscalar implementations. Where superscalar chips need hardware to scan the *****instruction***** stream looking for independent *****instructions***** that can be executed simultaneously, VLIW chips blindly fetch one wide *****instruction***** per cycle and execute all operations specified in the *****instruction*****. The processor can be this simple because the compiler performs operation scheduling normally done at run time in a superscalar processor. A VLIW microprocessor requires the compiler to perform static *****instruction***** scheduling; a superscalar machine performs dynamic *****instruction***** scheduling in hardware.

TriMedia = VLIW + DSP

The TriMedia architecture attempts to combine the benefits of VLIW and DSP architectures. The first generation has an *****instruction***** with up to five independent operations. If TriMedia were simply a five-wide VLIW, however...

...of general-purpose microprocessors. By the time TriMedia arrives, superscalar machines capable of executing five *****instructions***** per cycle will probably be fairly common (Even today, IBM's Power2 can execute six...

...similar to UltraSparc's PDIST - see page 16) and quadavg (sum of four rounded averages) *****instructions***** implement functions useful in MPEG decoding. These single-cycle *****instructions***** fetch two 32-bit

operands but operate on four pairs of bytes.

The peak performance of 2.5 billion operations/s is calculated as follows. Each TriMedia-1 *****instruction***** has up to five operation slots. Two of those slots can be filled with me8...

...single operation plus guard condition (explained below). Thus, the maximum number of primitive operations per *****instruction***** is 25 ($11 + 8 + 3 \times 2$). At 100 MHz, this yields the claimed peak performance.

This performance is dearly not the same as 2.5 billion *****instructions*****/s for a general-purpose microprocessor, but for TriMedia's intended ...triangles/s (texture-mapped, Gouraud shaded, [alpha]-blended, fogged, Z-buffered) with a 32-bit *****SDRAM***** interface or 250,000 triangles/s with 64-bit *****SDRAM*****. TriMedia-1 can also implement MPEG-2 decoding and the H.261 codec (coder/decoder...
...One of the things Philips learned from the LIFE experiment was that raw, verbose VLIW *****instructions***** are wasteful, especially in a machine with a large number of execution units. While the tight inner loops of performance-critical applications often result in full use of available *****instruction***** slots, no-ops must be inserted into some slots most of the time. The result is suboptimal use of bus bandwidth and *****instruction*****-cache capacity.

To combat this problem, TriMedia uses a modest (for a VLIW processor) *****instruction***** size - five operation slots - even though the first chip will implement 25 execution units. In...

...compression technique to avoid wasting space on no-ops.

Figure 4 shows the general TriMedia *****instruction***** format with its five operation slots. Each slot has six fields: an opcode, three register...

...is able to do good static branch prediction.

The actual binary encoding of a given *****instruction***** is not as simple as Figure 4 would suggest. *****Instructions***** are compressed by removing no-ops and encoding the most frequently occurring operations with the fewest bits. *****Instructions***** are byte aligned, and each *****instruction***** is described by a short header that tells how many operation slots are in used in the *****instruction***** and what encoding is used for each slot.

Hardware Rich in Execution Resources

Figure 5...

...compiler can use the large number of registers to implement the essential function of a *****reorder***** buffer (found in some superscalar implementations) without the hardware cost. This is another way that...

...TriMedia) is like a simplified superscalar processor. Instead of requiring hardware for dynamic scheduling of *****reorder*****-buffer entries, the compiler statically schedules the "*****reorder***** buffer" in a large number of registers.

Figure 6 shows a block diagram of the TriMedia-1 chip. Compared to a raw VLIW, TriMedia has extra hardware for the *****instruction***** -decompression logic, the operation-routing network, and the register-routing network. These circuits are not...

...generators, several integer ALUs, DSP execution units (to, for example, execute the me8 and quadavg *****instructions***** mentioned above), integer multipliers, integer shifters, branch units, load-store units, and floating-point units...

...has a branch delay of three cycles, requiring the compiler to generate three delay-slot *****instructions*****. To completely M1 this delay, the

compiler must find 15 useful operations.

Compiler Strategy

The...

12/3,KWIC/7 (Item 7 from file: 275)
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01631063 SUPPLIER NUMBER: 14363829 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Fast DRAMs can be swapped for SRAM caches. (dynamic/static random access
memory)(includes related article on Row Address Strobe) (Technical)
Bursky, Dave
Electronic Design, v41, n15, p55(8)
July 22, 1993
DOCUMENT TYPE: Technical ISSN: 0013-4872 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 4706 LINE COUNT: 00355

...ABSTRACT: are offered by Ramtron and Mitsubishi. Another innovation for
raising memory access times is the *****synchronous***** *****DRAM*****
which is presently under development at Samsung, Oki Semiconductors,
Fujitsu, Hitachi, Micron and Toshiba. However, *****SDRAM***** designers
have still to resolve their disagreement as to which of two schemes
performs better...

Diminishing processor *****instruction***** cycle times have forced
system designers to create faster memory subsystems to ensure that the CPU
almost never has to wait for the next *****instruction***** or data word.
In most current system designs, that means using a substantial amount of...
all of the on-chip timing for synchronous operation, also making this chip
the first *****synchronous***** *****DRAM***** that can deliver data in
10-ns/nibble bursts (16 nibbles per burst from the...

...transfer rates. The two data-transfer buffers can also be set to operate
in a *****sort***** of ping-pong mode so that a continuous data stream can
be delivered either to...

...available in 1994.

However, just as Ramtron and Mitsubishi came up with different
implementation approaches, *****SDRAM***** developers have split two
different ...far has only two DRAM suppliers--Samsung and Oki
Semiconductor. Most, if not all, other *****SDRAM***** suppliers have
indicated they will offer the JEDEC dual-bank pulsed-RAS versions such as
...

...bank, 16-Mbit memory soon to be released by Micron.

The JEDEC standard has four *****command*****-input pins--Chip Select,
RAS, CAS, and Write Enable. In the pulsed-RAS memories, the...

...just one-fourth the time currently needed by most of today's caches.

The Samsung *****SDRAM***** includes many features that help designers
at the system level. For example, built-in power...

...memories. The chip also bears a programmable CAS latency period. The
adjustable period allows the *****SDRAM***** to be used in any system,
regardless of operating frequency or bus-transfer speed.

To...

...and 2 by 512 kwords by 18 bits.

Fujitsu, Hitachi, Micron, Toshiba, and most other *****SDRAM*****

suppliers have adopted a JEDEC-compatible *****SDRAM***** architecture referred to as a prefetch approach by their memory designers. By employing the pre refresh-cycle SDRAMs.

The NEC *****SDRAM***** family offers yet another option that isn't part of the JEDEC standard--the memory...

...TTL (LVTTL) inputs to handle the lower operating voltages and smaller signal swings. NEC's *****SDRAM***** is the only one with dual, 3.3- or 5-V power-supply input capability...

...LVTTL and uses an 800-m V signal swing. A voltage-reference pin on their *****SDRAM***** can be used to set the desired interface. When grounded, the |V.sub.REF pin...

...SDRAMs, system timing operations are very straightforward thanks to the extensive definition of the four *****command***** inputs--Chip Select, RAS, CAS, and Write Enable. With each leading-edge tick of the 66.7-to-100-MHz clock, the state of the *****command***** inputs determines the operation the *****SDRAM***** must perform--a burst read or a burst write, no operation, precharge, and so on...

...When a host requests data or wants to write data, it sends a Request Packet *****command***** to the RDRAMs. It then reads or writes up to 256 bytes. A packet request...the Chip Select pin at the system level. Thus, to design a controller for both *****SDRAM***** styles, the output *****SDRAM***** controller pin that selects the banks should drive RAS on one bank and CS on two banks.

Furthermore, the JEDEC *****SDRAM***** standard provides for either an |A.sub.11

address input or a Bank Address (BA...

...A.sub.11

nomenclature refers to the most-significant-address bit of a one-bank *****SDRAM***** , while two-bank SDRAMs use a BA signal to select the internal bank. This distinction is key to understanding the *****SDRAM***** differences. In single-bank SDRAMs, the |A.sub.11 pin must be valid only when...

...not only while activating a new row address, but also during Read, Write, and Precharge *****commands*****. By designing for one bank and reasserting the |A.sub.11

input during Read and Write cycles, an *****SDRAM***** controller can support both types of SDRAMs.

Unfortunately, even among dual-bank SDRAMs, competing architectures...

...prefetch architecture" that limits random column addresses to every other clock cycle. As a result, *****SDRAM***** controllers designed for maximum flexibility should avoid back-to-back random column address cycles.

12/3,KWIC/8 (Item 1 from file: 624)
DIALOG(R)File 624:McGraw-Hill Publications
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0670984

FAST, SMART RAM: Memory chips are getting faster and more capable but not less expensive. BYTE *****sorts***** out the new types of RAM--what each is good for, and which ones you're likely to see on your next PC.

BYTE June, 1995; Pg 187; Vol. 20, No. 6

Journal Code: BYTE

ISSN: 0360-5280

Section Heading: State of the Art

Word Count: 3,453 *Full text available in Formats 5, 7 and 9*

BYLINE:
PETER WAYNER

: Memory chips are getting faster and more capable but not less expensive.
BYTE *****sorts***** out the new types of RAM--what each is good for,
and which ones you...

TEXT:
... the marketplace. Many system integrators and RAM manufacturers agree
that the price differential that EDORAM *****commands***** will evaporate
by early 1996.

The technology behind EDORAM is a simple extension of the...is a cleaner
replacement for the old interfaces between chips. Normally, memory chips
answer requests. *****SDRAM***** (*****synchronous***** *****DRAM*****)
feeds off the same clock cycle as the CPU, anticipating the CPU's demands
and...

... present the data for output. Many people predict that 1996 will be the
year of *****SDRAM***** , because 66-MHz or higher CPUs will be common by
then and will need *****SDRAM*****. Until then, however, *****SDRAM*****
will *****command***** a 20 percent to 50 percent premium over commodity
DRAM. Also, the price of these...

...systems must cover the added cost of the different logic chips needed to
drive the *****SDRAM*****.

Another way to speed memory access is by adding an on-chip cache. This
approach...

...continuing to examine packages that might offer a more stable and faster
bus. For instance, *****SDRAM***** requires that the RAM and the CPU share
clocking information, and more precise packaging may...

... even edge of the clock cycle. This synchronization is similar to the
process proposed for *****SDRAM*****. All these factors combine to enable
transfer speeds up to 500 MBps.

VRAM

The commodity... all be used to increase the speed of the RAM on video
boards. EDORAM, CDRAM, *****SDRAM***** , and other DRAM enhancements can be
substituted on the board quickly and effectively. In addition...

TABLE:
...EDOVram extended data out VRAM
FPM fast page mode
FRAM ferroelectric RAM
RDRAM Rambus DRAM
*****SDRAM***** *****synchronous***** *****DRAM*****
SRAM static RAM
SVRAM synchronous VRAM
3D RAM Matsushita's chip for 3-D video...

12/3,KWIC/9 (Item 1 from file: 9)
DIALOG(R)File 9:Business & Industry(TM)
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01466095 (USE FORMAT 7 FOR FULLTEXT)

M'soft sends PC message

(Microsoft Corp unveils Simply Interactive PC Platform, distributes hardware recommendations)

Electronic Engineering Times, p 1+

April 08, 1996

DOCUMENT TYPE: Journal ISSN: 0192-1541

LANGUAGE: English RECORD TYPE: Fulltext

WORD COUNT: 1858

(USE FORMAT 7 FOR FULLTEXT)

ABSTRACT:

...digital surround-sound audio; MPEG and sound functions run on Intel Corp's MMX X86-*****instruction*****-set extensions; MPEG-2 and AC-3 for DVD players; 16Mbyte *****SDRAM***** or SGRAM main memory; and quality L2 caches on systems that support multimedia and multitasking...

TEXT:

...Gates said in the interview. "Everything we talk about under the SIPC banner is just *****sort***** of the first phase of what we need to do."

Microsoft and Intel Corp. have...

...surround-sound audio;

prepare to run MPEG and sound functions on Intel's MMX X86-
*****instruction*****-set extensions;

prepare to support MPEG-2 and AC-3 for DVD players;

plan for 16-Mbyte *****SDRAM***** or SGRAM main memory;

keep quality L2 caches in systems to support multimedia and multitasking...

12/3,KWIC/10 (Item 1 from file: 636)

DIALOG(R)File 636:IAC Newsletter DB(TM)

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02932164

GRAPHICS COMMUNICATION LABORATORIES: First MPEG2 MPoML/HI, VideoEncoder
ChipSet developed in Tokyo

M2 Presswire Oct 10, 1995

WORD COUNT: 860

PUBLISHER: M2 Communications

...LTD ; M2 PRESSWIRE 10 October 1995 GRAPHICS COMMUNICATION LABORATORIES ;
Nippon Telegraph and Telephone Corporation ; Reduced *****Instruction*****
Sets Computer ; Tokyo Graphics Communication Laboratories

...262 (MPEG2 Video) MP@ML/HL.

2. One VLSI ChipSet of five chips and three *****SDRAM***** (
*****synchronous***** *****dynamic***** *****random***** *****access*****
*****memory*****) chips offers real-time encoding at MP@ML level.
M@HL(HI)TV) can be...

... main level video, including preprocessing for video signal, with only

five VLSI chips and three *****SDRAM***** chips.
High-quality picture encoding by using GCL-developed algorithm A
RISC(Reduced *****Instruction***** Sets Computer) installed in the QVL chip
implementing a GCL-developed algorithm achieves high-quality...

...ChipSet

LSI	FUNCTION
PRE	Prefiltering, Format Conversion (4:2:2 to 4:2:0, SIF), *****Reordering***** of Frames, CME Chip Control, Memory Control
CME	Coarse Motion Estimation
FME	Fine Motion Estimation...

12/3,KWIC/11 (Item 1 from file: 16)
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05894104

Trade-offs key, as chip sets take center stage

Electronic Engineering Times Nov 13, 1995 p. 92
ISSN: 0192-1541
FULL TEXT AVAILABLE IN FORMAT 7 OR 9 WORD COUNT: 1309

... disk-drive performance boost-are such that virtually all chip- set
vendors now offer some *****sort***** of support for the Bus Master IDE
mode.

Integration is an issue in that some...

... flat pack (PQFP) implementations. But while BGAs may offer improvements
in motherboard assembly yields, they *****command***** a premium and face
supply constraints that have hampered more widespread adoption of BGA
packaging...

...bit-wide main memory, UMA can take advantage of the new and faster DRAMs
(EDO, *****synchronous***** *****DRAM***** , etc.) while bypassing the
32-bit constraints of the PCI bus. In the long run a non-UMA design that
employs *****synchronous***** *****DRAM***** and top-of-the-line 133-MHz
processors. But UMA is particularly valuable because it...

12/3,KWIC/12 (Item 2 from file: 16)
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05894097

Designing Computers

...in most designs is the memory subsystem.

The time needed to access or fetch an *****instruction***** is largely dependent on the memory system. Memory access time will continue to be the ...

... RISC designs help reduce memory-bandwidth requirements, achieving a completion rate of one or more *****instruction***** per cycle-the rate that has become the norm in most advanced CPU designs-is impossible unless the memory subsystem can deliver the *****instructions***** at the clock rate of the processor. In many of the newer CPUs-almost all...

... address strobe (CAS) cycle-time delay. Burst accesses allow the system logic to provide data/*****instructions***** from memory locations within only the CAS cycle time. The burst throughput can thus be increased and the processor's pipeline and *****instruction***** queues filled sufficiently.

But as memory access time-both row-address strobe (RAS) and column...

... prefetch queue's being flushed. That holds especially true for cases in which the required *****instruction***** extends beyond the first double word of the burst. In such a case, the CPU...

... additional potential performance inhibitors. They have to do with the fact that in the Pentium, *****memory***** *****requests***** come primarily from these sources: direct requests from the execution unit; indirect requests from other...

... requests on behalf of those other functions, indentifying the source, type and length of the *****memory***** *****request***** by a unique set of signals.

Application dictates

The delay and wait states with which...

... For a word processor such as Word operating under Windows 3.1, the number of *****memory***** *****requests***** can be between 4 million and 5 million per second, depending on the kind of...

...one finds that as much as 40 percent of the CPU workload is dominated by *****instruction***** fetches and data writes from the write buffer, with the rest divided ...can push it on the controller side," warned Ng of Oak Technology. "After that, all *****sorts***** of things get in the way: noise, due to the number of pins switching and...

... Via . "The problem now is to find out which of the alternative DRAMs-burst EDO, *****SDRAM***** or, possibly, cache or enhanced DRAM-not only have the necessary bandwidth but also do something to mask the inherent latency of DRAMs."

Hedging bets

As system designers *****sort***** through the alternatives, core-logic vendors are hedging their bets by supporting as many of...

... level caching or find some alternative." Simply going to higher performance DRAM alternatives, such as *****SDRAM***** or burst EDO, will not suffice.

Some of the new UMA core-logic chip sets...by a burst from the system, the CPU doesn't need constant memory access for *****instructions***** and data.

"However, increasing the CPU cache size with relatively more expensive SRAM offsets the...

... rumored to have a second-level cache on board, as well as so-called visual *****instructions*****, similar in function to those proposed by Sun for its Ultrasparc CPU.

Even further ahead...

12/3,KWIC/13 (Item 3 from file: 16)
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05486905

MPUs take on DSP's role

Microprocessor chips are ready to take on Digital Signal Processing functions

Electronic Engineering Times October 31, 1994 p. 28

ISSN: 0192-1541

FULL TEXT AVAILABLE IN FORMAT 7 OR 9 WORD COUNT: 2217

... keep up with audio-grade DSP chips by itself. And the fact that all ARM *****instructions***** are conditional permits very tight coding of the inner loops that characterize DSP code. "For...

...At this point, we don't see enough agreement in the industry to do the *****sort***** of dedicated execution unit that, for instance, Ultrasparc has."

... pipeline to support a multiply followed by an add. In effect, we fold that add *****instruction*****, so it is there in the code but doesn't take excess cycles. The code...

...runs faster."

MIPS won't be the only company taking this approach with the MIPS *****instruction***** set. Integrated Device Technology (IDT), which has struck out on its own with the MIPS...

... maximum value instead of wrapping around when an overflow occurs. "The saturation add replaces nine *****instructions***** that would be needed to do the same operation on two 16-bit quantities in the standard PA-RISC *****instruction***** set," Mahon observed.

Because the changes to the hardware were all off the critical paths...

...to assert itself. It's fine to be able to do lots of multiply-accumulate *****instructions***** in a clock cycle, but if you can't get the video stream in and... effective to hose large blocks of data directly onto the chip through something like a *****synchronous***** *****DRAM***** interface, and then hose it back out again.

The PA-RISC architecture recognizes this fact...

12/3,KWIC/14 (Item 4 from file: 16)
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05202781

Rambus gets design win

Unveils new game system that uses Rambus DRAM chip

Electronic Engineering Times July 18, 1994 p. 25

ISSN: 0192-1541

FULL TEXT AVAILABLE IN FORMAT 7 OR 9 WORD COUNT: 1195

... line synchronous bus clocked at 500 MHz. It uses a message-passing format to pass *****commands***** or data in bursts. R (for Rambus) DRAMs are designed to complement the bus. The RDRAM chips are organized internally like conventional DRAMs, but use their sense amps as a *****sort***** of cache. So when an RDRAM reads, it transfers an entire row of data to...

...memory system, you have two choices. If you use conventional memory tech or the new *****SDRAM***** parts, to get to that level you have to use multiple parts in parallel and...

12/3, KWIC/15 (Item 5 from file: 16)
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04418444
PDAs challenge MPU makers

Electronic Engineering Times April 26, 1993 p. 90
ISSN: 0192-1541
FULL TEXT AVAILABLE IN FORMAT 7 OR 9 WORD COUNT: 2398

...maybe 90 percent correct responses. For electronic ink, that's fine. But for data and *****command***** entry, that's not acceptable. We need a quantum jump in either CPU speed or...to accomplish that. Several vendors reported investigating low-swing serial buses - using either Rambus or *****synchronous***** *****DRAM***** interfaces - as a way of reducing the bus power dissipation. 'You have to balance power...

...in the CPU chip, reducing both parts count and external bus cycles. Finally, key DSP *****instructions***** , such as the multiply/accumulate, can be integrated into the CPU core on the RISC...

... hardware on the chip, the die size grows enormously. If you just integrate a MAC *****instruction***** , extra hardware is minimal. That will get you low-level voice recognition, sound generation and...own silicon solution.

But that raises a small question of methodology. Are the new chips *****sort*****-of-standard products that wind up in a vendor's catalog? Are they full ASICs...

...top-down, full-custom methodology, backed by sophisticated design tools. You can't approach this *****sort***** of design with conventional ASIC tools, which focus on assembling and wiring tasks instead of...

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File 47:Magazine Database(TM) 1959-1996/May 10
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File 75:IAC Management Contents(R) 86-1996/May W1
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Set	Items	Description
S1	1339	SDRAM OR SYNCHRON?() (DRAM OR (DYNAMIC() (RAM OR RANDOM() ACC- ESS() (MEMORY OR MEMORIES))))
S2	32	(SORT? REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR COMM- AND? ? OR MEMORY()REQUEST? ?)
S3	4415	(SORT? OR REORDER? OR RE()ORDER?) (10N) (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S4	0	S1 AND S2
S5	8	S1 AND S3
S6	66425	(SORT? OR REORDER? OR RE()ORDER?) AND (INSTRUCTION? ? OR C- OMMAND? ? OR MEMORY()REQUEST? ?)
S7	31	S1 AND S6
S8	1066	(ADDRESS? OR LOCATION?) (100N) (OUT(1W) (ORDER OR SEQUENCE OR PLACE OR TURN))
S9	5	S1 AND S8
S10	6	RD S5 (unique items)
S11	23	S7 NOT S5
S12	15	RD S11 (unique items)
S13	2	S9 NOT (S5 OR S7)
S14	1	RD S13 (unique items)

14/3,KWIC/1 (Item 1 from file: 275)
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01710873 SUPPLIER NUMBER: 16184759 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Digital leads the pack with 21164; first of next-generation RISCs extends
Alpha's performance lead. (includes related articles on DEC's 21171 chip
set and the price and availability of the 21164 and 21171) (Product

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(FILE 'USPAT' ENTERED AT 11:26:58 ON 10 MAY 96)

L1 48 S SYNCHRONOUS?(3W)DRAM
L2 424 S (SORT OR SORTED OR SORTING) (3A)ADDRESS?
L3 271 S PRIORIT?(4A) (MEMORY(3A)REQUEST?)
L4 0 S ((RE(W)ORDER?) OR REORDER?) (3A) (MEMORY(2W)REQUEST?)
L5 0 S L1 AND L3
L6 0 S L1 AND L2
L7 649 S SORTING(2A) (UNIT OR MEANS OR PORTION)
L8 0 S L1 AND L7
L9 29742 S SCHEDUL?
L10 0 S L1 AND L9
L11 19 S L1(P) (CONTROL OR CONTROLLER)
L12 0 S L2(P)L3
L13 9 S L2(P)L7
L14 662 S PIPELIN?(3A) (DRAM OR MEMORY)
L15 53 S SYNCHRON?(2W)DRAM
L16 23 S L15(P) (CONTROL OR CONTROLLER)
L17 26 S (TAG OR TAGGING) (3A) (MEMORY(3A)REQUEST?)
L18 5 S L17 AND (SORT OR SORTING OR SCHEDUL?)
L19 2706 S MEMORY(2W)REQUEST? .
L20 206293 S TAG OR TAGGING OR MARK OR MARKED OR MARKING
L21 11 S L20(3W)L19
L22 29 S INDICAT?(3A) ((SENDING OR SEND OR ACCESS?) (2A)ORDER?)
L23 0 S L21(2P)L22
SAVE A437975/L ALL
L24 2327 S DIVIDING(3A)CLOCK
L25 14190 S OUT(3W)ORDER
L26 0 S L25(3W)L19

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1. 5,513,148, Apr. 30, 1996, ****Synchronous** NAND **DRAM** architecture;**
Paul Zagar, 365/233, 230.09, 236 [IMAGE AVAILABLE]

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5. 5,381,536, Jan. 10, 1995, Method and apparatus for separate mark and
wait instructions for processors having multiple memory ports; Andrew E.
Phelps, et al., 395/375; 364/262.9, 263, 946.7, 973, DIG.1, DIG.2 [IMAGE
AVAILABLE]

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